ST.ANNE'S COLLEGE OF ENGINEERING AND TECHNOLOGY

ANGUCHETTYPALAYAM, PANRUTI-607 110.

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

EC 8311 ELECTRONICS LABORATORY

II YEAR / III SEMESTER ELECTRICAL AND ELECTRONICS ENGINEERING

PREPARED BY :
Ms. J. ARUL MARTINAL, AP/EEE

LIST OF EXPERIMENTS

1. Characteristics of Semi conductor diode and Zener diode
2. Characteristics of a NPN Transistor under common emitter , common collector and common base configurations
3. Characteristics of JFET(Draw the equivalent circuit)
4. Characteristics of UJT and generation of saw tooth waveforms
5. Design and Frequency response characteristics of a Common Emitter amplifier
6. Characteristics of photo diode & photo transistor, Study of light activated relay circuit
7. Design and testing of RC phase shift, LC oscillators
8. Single Phase half-wave and full wave rectifiers with inductive and capacitive filters
9. Differential amplifiers using FET
10. Study of CRO for frequency and phase measurements
11. Astable and Monostable multivibrators
12. Realization of passive filters

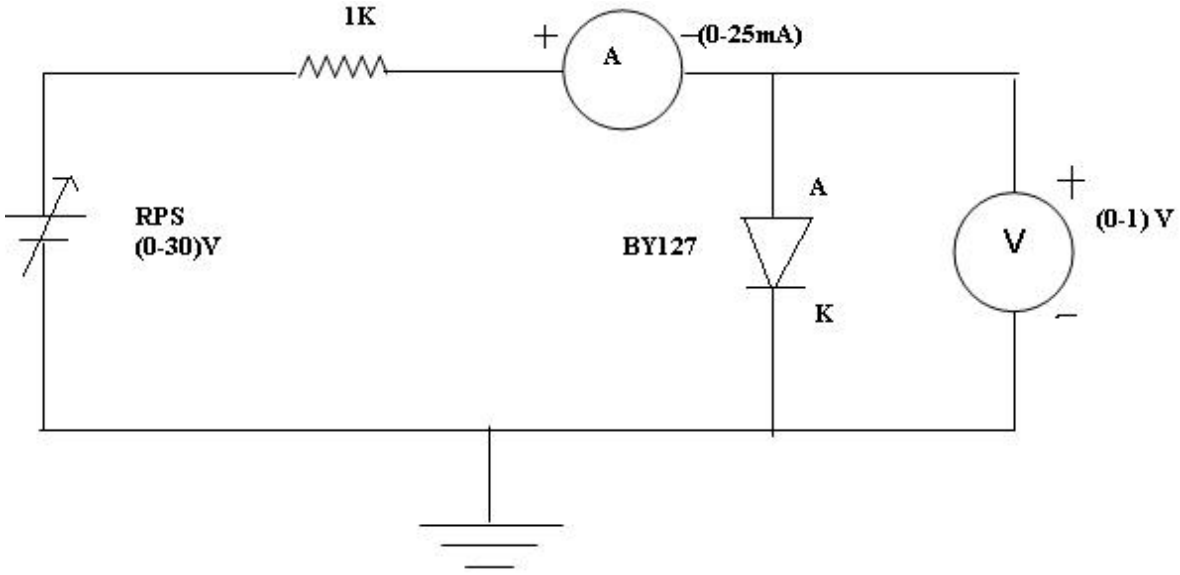
ADDITIONAL EXPERIMENTS (TOPIC BEYOND SYLLABUS)

1. Tuned class C Amplifier
2. Bistable

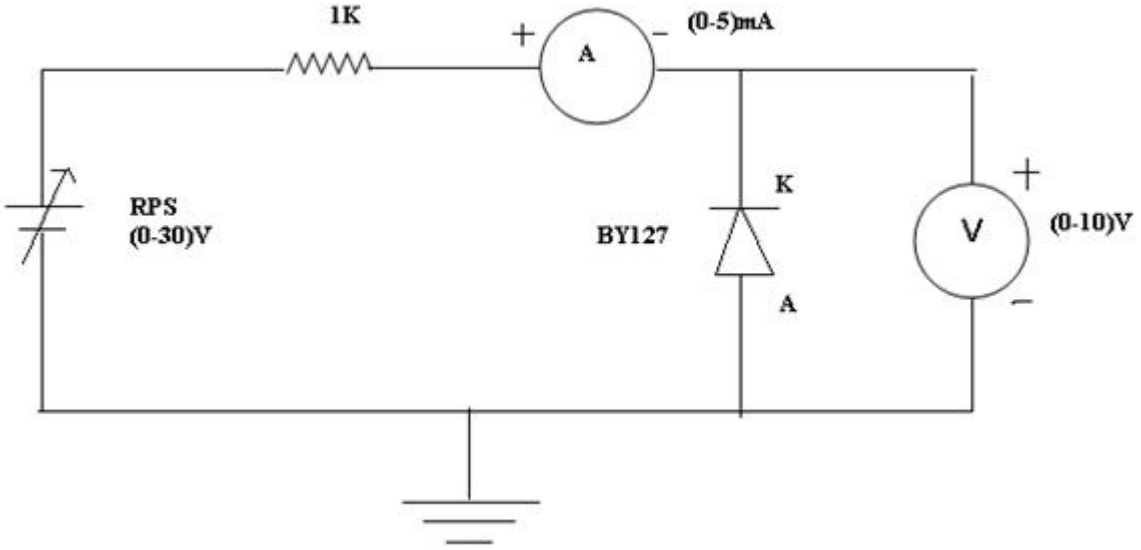
Multivibrator

CIRCUIT DIAGRAM:

FORWARD BIAS:



REVERSE BIAS:



EX.NO : 1 a.

CHARACTERISTICS OF SEMICONDUCTOR (PN JUNCTION) DIODE

AIM:

To determine the VI characteristics of PN Diode

APPARATUS REQUIRED:

S.No	Name	Range	Type	Qty
1	R.P.S	(0-30)V		1
2	Ammeter	(0-100)μA, (0-25) mA		2 1
3	Voltmeter	(0-10)V (0-1)V		1 1
4	Connecting wires			
5	Bread Board			1
6	Resistors	1KΩ		2
7	Diode- PN	BY127		1

THEORY:

A diode is a PN junction formed by a layer of P type and layer of N type Semiconductors. Once formed the free electrons in the N region diffuse across the junction and combine with holes in P region and so a depletion Layer is developed. The depletion layer consists of ions, which acts like a barrier for diffusion of charged beyond a certain limit. The difference of potential across the depletion layer is called the barrier potential. At 2.5degree the barrier potential approximately equal 0.7v for silicon diode and 0.3v for germanium diode.

When the junction is forward bias, the majority carrier acquired sufficient energy to overcome the barrier and the diode conducts. When the junction is reverse biased the depletion layer widens and the barrier potential increases. Hence the Majority carrier cannot cross the junction and the diode does not conduct. But there will be a leakage current due to minority carrier. When diode is forward biased, resistance offered is zero, and when reverse biased resistance offered is infinity. It acts as a perfect switch.

TABULATION:

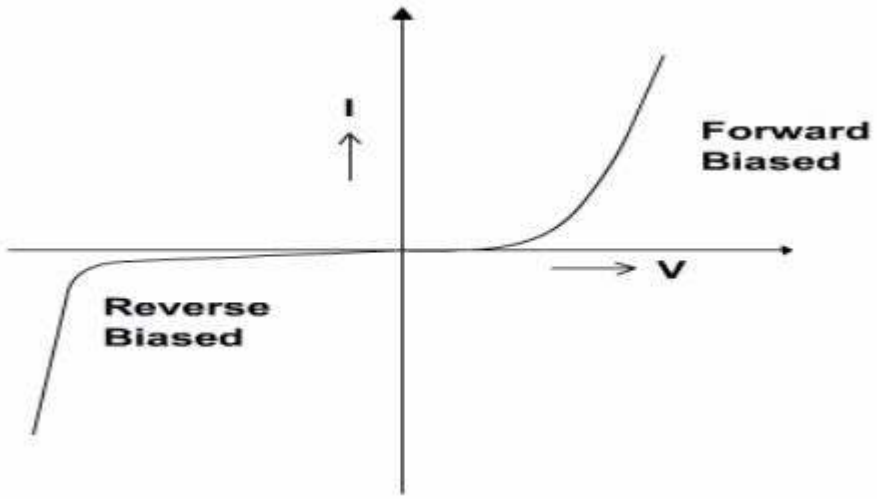
FORWARD BIAS:

V_f(volts)	I_f(mA)

REVERSE BIAS:

V_r(volts)	I_r(mA)

MODEL GRAPH



PROCEDURE:

FORWARD BIAS:

1. The connections are made as per the circuit diagram.
2. The positive terminal of power supply is connected to anode of the diode and negative terminal to cathode of the diode.
3. Forward voltage V_f across the diode is increased in small steps and the forward current is noted.
4. The readings are tabulated. A graph is drawn between V_f and I_f.

REVERSEBIAS :

1. The connections are made as per the circuit diagram.
2. The positive terminal of power supply is connected to cathode of the diode and negative terminal to anode of the diode.
3. Reverse voltage V_f across the diode is increased in small steps and the Reverse current is noted.
4. The readings are tabulated. A graph is drawn between V_r and I_r.

REVIEW QUESTIONS:

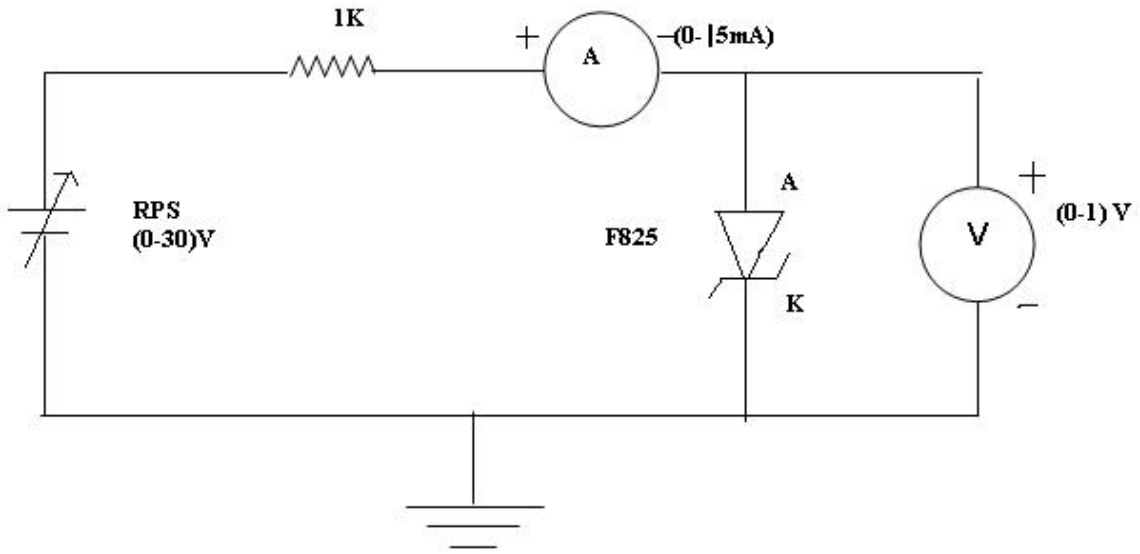
1. How a PN junction is formed?
2. In what way the width of depletion region can be varied?
3. What is potential barrier?
4. In forward bias condition the current condition is due to_____
5. What is reverse saturation current Ico?
6. How diodes act as switch?
7. What is Dynamic Resistance?
8. Why it is called DIODE?
9. What are the majority carriers of P-Type and N-Type semiconductor?

RESULT:

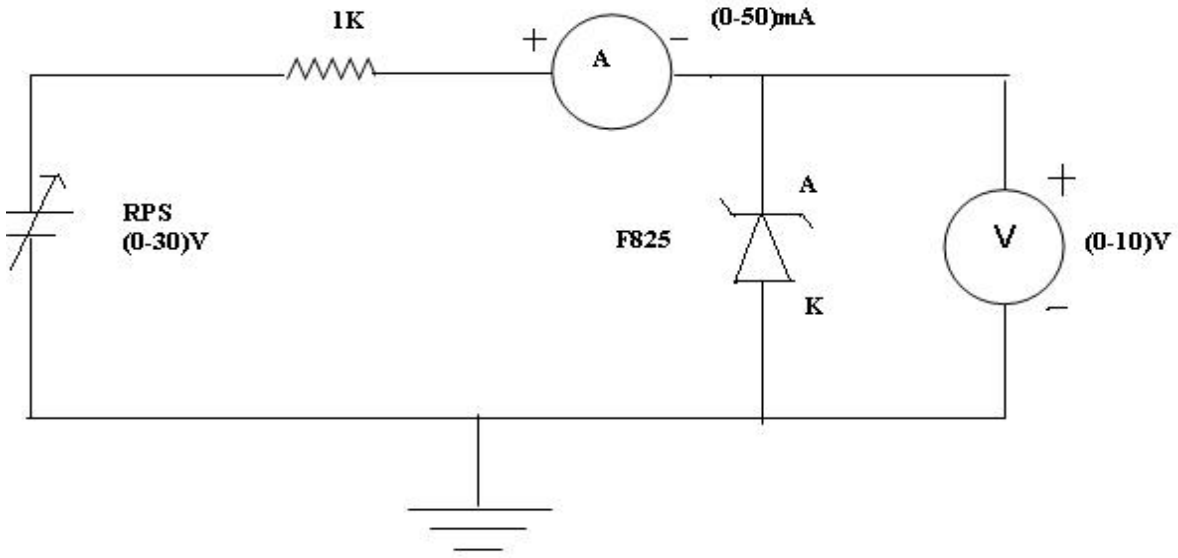
Thus the characteristics of PN-Junction diode were drawn.

CIRCUIT DIAGRAM:

FORWARD BIAS:



REVERSE BIAS:



EX. NO: 1(b)

CHARACTERISTICS OF ZENER DIODE

AIM:

To determine the VI characteristics of Zener Diode

APPARATUS REQUIRED:

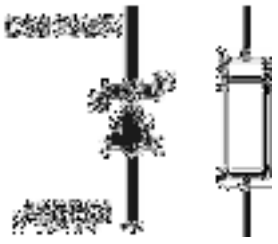
S.No	Name	Range	Type	Qty
1	R.P.S	(0-30)V		1
2	Ammeter	(0-15) mA (0-50) mA		1 1
3	Voltmeter	(0-10)V (0-1)V		1 1
4	Connecting wires			
5	Bread Board			1
6	Resistors	1KΩ		2
7	Diode- Zener	F825		1

THEORY:

Zener diodes have many of the same basic properties of ordinary semiconductor diodes. When forward biased,they conduct in the forward direction and have the same turn on voltage as ordinary diodes. For silicon this is about 0.6 volts.

In the reverse direction, the operation of a Zener diode is quite different to an ordinary diode. For low voltages the diodes do not conduct as would be expected. However, once a certain voltage is reached the diode "breaks down" and current flows. Looking at the curves for a Zener diode, it can be seen that the voltage is almost constant regardless of the current carried. This means that a Zener diode provides a stable and known reference voltage. Hence they are used as Voltage regulators.

PIN DIAGRAM:



TABULAR COLUMN:

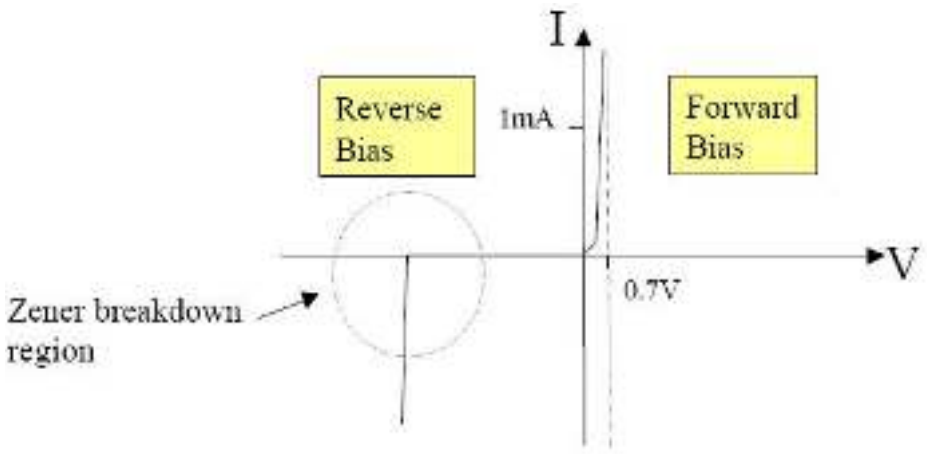
FORWARD BIAS:

V_f(volts)	I_f(mA)

REVERSE BIAS:

V_r(volts)	I_r(mA)

MODEL GRAPH



PROCEDURE:

FORWARD BIAS:

1. The connections are made as per the circuit diagram.
2. The positive terminal of power supply is connected to anode of the diode and negative terminal to cathode of the diode.
3. Forward voltage V_f across the diode is increased in small steps and the forward current is noted.
4. The readings are tabulated. A graph is drawn between V_f and I_f.

REVERSEBIAS:

1. The connections are made as per the circuit diagram.
2. The positive terminal of power supply is connected to cathode of the diode and negative terminal to anode of the diode.
3. Reverse voltage V_f across the diode is increased in small steps and the Reverse current is noted.
4. The readings are tabulated. A graph is drawn between V_r and I_r.

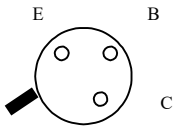
REVIEW QUESTIONS:

1. How Zener diode acts as a voltage regulator.
2. Explain working of a Zener Diode
3. What is the cut-in voltage of zener diode?
4. Differentiate between Zener Breakdown and Avalanche breakdown
5. Why zener diode is often preferred than PN diode
6. List the application of zener diode
7. Define zener breakdown voltage
8. Define Zener diode

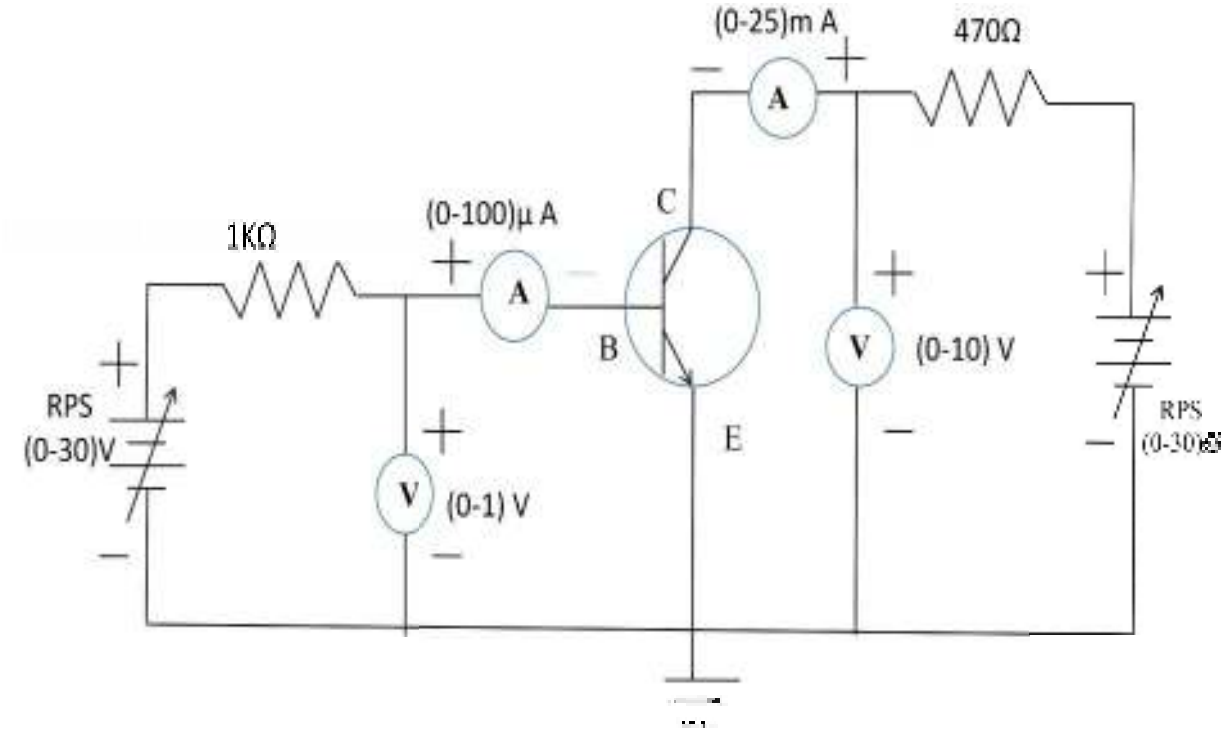
RESULT:

Thus the characteristics of Zener diode were drawn**.**

PIN DIAGRAM OF BC107



CIRCUIT DIAGRAM:



EX.NO:2a

CHARACTERISTICS OF NPN TRANSISTOR UNDER CE CONFIGURATION

AIM:

To plot the transistor characteristics (INPUT & OUTPUT) of CE configuration .

APPARATUS REQUIRED:

S.No.	COMPONENTS	SPECIFICATION	QTY
1	Transistor BC 107	Max Rating : 50V 1A, 3W	1
2	Resistors	1kΩ,470Ω	2
3	Regulated power supply	(0-30) V	1
4	Voltmeters	Mc (0-10) v Mc (0-1) v	1 1
5	Ammeters	Mc (0-10) m A	2
6	Bread board & connecting wires		

THEORY:

A NPN function transistor consist of a silicon (or germanium) crystal in which a layer of p – type silicon is sandwiched between two layers of N – type silicon. The arrow on emitter lead specifies the direction of the current flow when the emitter – base function is biased in the forward direction since the conductivity of the BJT depends on both the majority and minority carriers it is called bipolar device. In CE configuration, Emitter is common to both the Emitter and Base.

TABULATION:

Input Characteristics:

V_{CE} = 1V		V_{CE} = 2V	
$V_{BE(V)}$	$I_{B\ (mA)}$	$V_{BE(V)}$	$I_{B(mA)}$

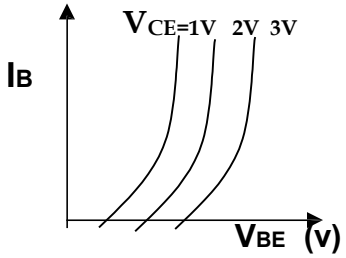
Output characteristics:

I_B = I_B=

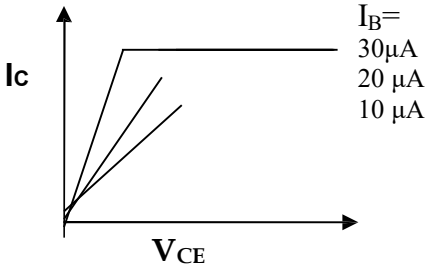
$V_{CE(V)}$	$I_{C\ (mA)}$	$V_{CE(V)}$	$I_{c\ (mA)}$

MODEL GRAPH:

INPUT CHARACTERISTICS



OUTPUT CHARACTERITICS



DESCRIPTION:

Input Characteristics:

Voltage across Base Emitter junction V_{BE} vs I_B, where V_{CE} constant

Output Characteristics:

Voltage across Collector Emitter junction V_{CE}vs $I_C$where I_B constant

PROCEDURE:

Input Characteristics:

1. Connections are made as per the circuit diagram.
2. V_{CE} is kept const (say 2v), V_{BE} is varied insteps of 0.1v and the corresponding I_B values are tabulated. The above procedure is repeated for 1V etc.
3. Graph is plotted between V_{BE} vs I_B, where V_{CE} constant.

Output Characteristics:

1. Connection are made as per the circuit diagram
2. I_B is kept const, V_{CE} is varied in step IV the corresponding I_C values are tabulated. The above procedure is repeated for different constant values.
3. Graph is plotted between V_{CE} and Ic for a constant I_B.

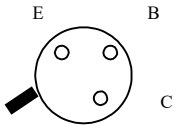
REVIEW QUESTIONS:

1. Explain the operation of CE configuration
2. Determine the output resistance and input resistance
3. Why BJT is called current controlled device?
4. Give some applications of BJT.
5. Among CE, CB, CC which one is most popular. Why?

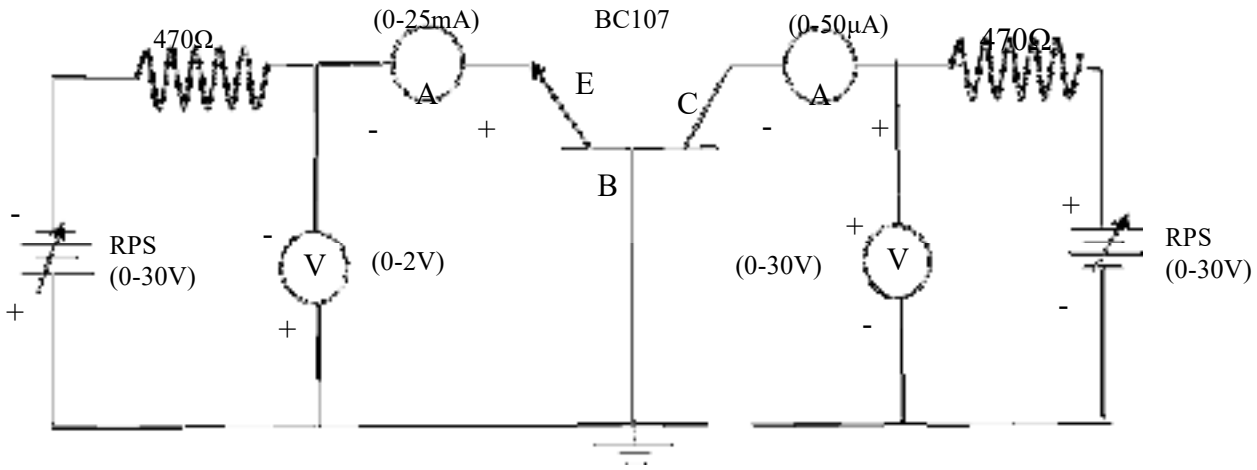
RESULT:

Thus the input and output characteristic of BJT in Common Emitter mode is drawn.

PIN DIAGRAM OF BC107



CIRCUIT DIAGRAM :



EX.NO:2b

CHARACTERISTICS OF NPN TRANSISTOR UNDER CB CONFIGURATION

AIM:

To plot the transistor characteristics (INPUT & OUTPUT) of CB configuration .

APPARATUS REQUIRED:

S.No.	COMPONENTS	SPECIFICATION	QTY
1	Transistor BC 107	Max Rating : 50V 1A, 3W	1
2	Resistors	1kΩ,470Ω	2
3	Regulated power supply	(0-30) V	1
4	Voltmeters	Mc (0-10) v Mc (0-1) v	1 1
5	Ammeters	Mc (0-10) m A	2
6	Bread board & connecting wires		

THEORY:

A NPN function transistor consist of a silicon (or germanium) crystal in which a layer of p – type silicon is sandwiched between two layers of N – type silicon. The arrow on emitter lead specifies the direction of the current flow when the emitter – base function is biased in the forward direction since the conductivity of the BJT depends on both the majority and minority carriers it is called bipolar device. In CB configuration,base is common to both the emitter and collector.

TABULATION:

Input Characteristics:

V_{CB} = 1V		V_{CB} = 2V	
$V_{BE(V)}$	$I_{E\ (mA)}$	$V_{BE(V)}$	$I_{E\ (mA)}$

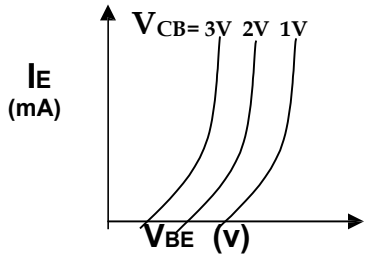
Output Characteristics:

I_E = 1mA I_E= 2mA

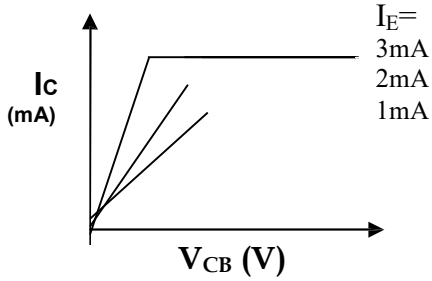
$V_{BE(V)}$	$I_{C\ (mA)}$	$V_{BE(V)}$	$I_{c\ (mA)}$

MODEL GRAPH:

INPUT CHARACTERISTICS



OUTPUT CHARACTERITICS



DESCRIPTION:

Input Characteristics:

Voltage across Base Emitter junction V_{BE} vs I_E, where V_{CB} constant

Output characteristics:

Voltage across Collector Emitter junction V_{BC}vs $I_C$where I_E constant

PROCEDURE:

Input Characteristics:

1. Connections are made as per the circuit diagram.
2. V_{CB} is kept const (say 2v), V_{BE} is varied insteps of 0.1v and the corresponding I_E values are tabulated. The above procedure is repeated for 1V etc.
3. Graph is plotted between V_{BE} vs I_E, where V_{CB} constant.

Output Characteristics:

1. Connection are made as per the circuit diagram
2. I_E is kept const, V_{BC} is varied in step IV the corresponding I_C values are tabulated. The above procedure is repeated for different constant values.
3. Graph is plotted between V_{BC} and Ic for a constant I_E.

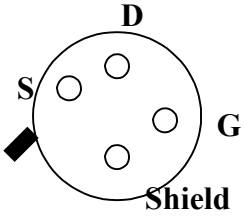
REVIEW QUESTIONS:

1. Bring out the comparison of CC, CE, and CB transistor parameters
2. Give the relation of Ebers moll equation.
3. In a bipolar transistor which region is wider and which region is thinner? Why?
4. What is thermal runaway?
5. State the relation between α and β of a transistor?

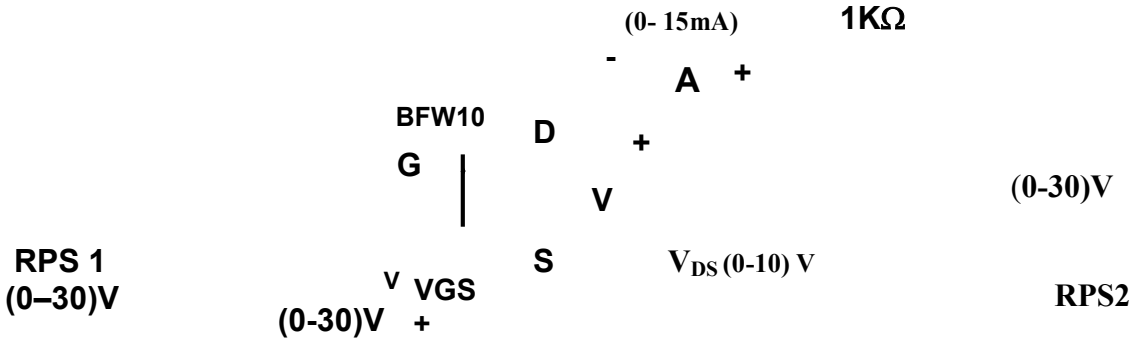
RESULT:

Thus the input and output characteristic of BJT in Common Base mode is drawn.

PIN DIAGRAM OF BFW10



CIRCUIT DIAGRAM



EX .NO-3

CHARACTERISTICS OF JFET

AIM:

To plot the drain and transfer characteristics of JFET & to find drain resistance, tran sconductance, amplification factor, drain saturation current I_{DSS} and Pinch off voltage.

APPARATUS REQUIRED:

S.No.	Components	Specification	Qty
1	FET	BFW10 I_{dss}> 8 mA, Vp<8V	1
2	Resistors	1kΩ	1
3	Regulated dual power supply	MC (0-30)V	1
4	Voltmeters	MC (0-10)V	2
5	Ammeters	MC (0-15) mA	1
6	Bread board & connecting wires		

THEORY:

Field effect transistor is a semiconductor device that depends for its operation on the control of current by an electric field. It's operation depends on the flow of majority carriers only. It is therefore a unipolar device. It exhibits a high input resistance. An N- channel JFET consists of a N-type bar is sandwiched between two heavily doped Persians. Due to the concentration gradient, the depletion region formed. On both sides of the semiconductor bar the ohmic contacts are made. One terminal is called source & other is called drain. Both the p-type regions are connected together.

TABULAR COLUMN:

Drain characteristics

V_{GS} = **-2V** V_{GS} = **-4 V**

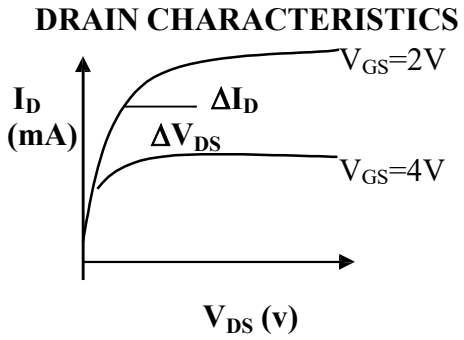
V_{DS} (V)	I_D (mA)	V_{DS} (V)	I_D (mA)

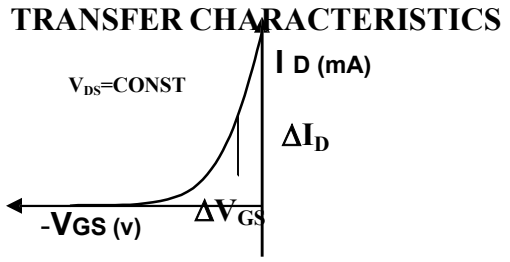
Transfer characteristics

V_{DS} = 2V V_{DS} =4V

V_{gs} (V)	I_D (mA)	V_{GS} (V)	I_D (mA)

MODEL GRAPH:





CALCULATION

Transconductance g_m = $\Delta I_D / \Delta V_G$

Drain resistance r_d = $\Delta V_{DS} / \Delta I_D$

Amplification factor $\mu = g_m r_d$

DESCRIPTION:

DRAIN CHARACTERISTICS

INPUT: Drain voltage V_{DS} is varied insteps of 1V, V_{GS} is kept constant

OUTPUT: Drain current I_D

TRANSFER CHARACTERISTICS

INPUT: Gate – source voltage V_{GS} is varied ,Drain –source voltage V_{DS} is kept constant

OUTPUT: Drain current I_D

PROCEDURE:

Drain Characteristics:

1. Connections are made as per the circuit diagram.
2. Gate –source voltage V_{GS} is kept constant (say –1v), drain voltage V_{DS} is varied insteps of 1v and the corresponding drain current I_D values are tabulated.
3. The above procedure is repeated for V_{GS}= -2v, 0v.
4. The graph is plotted V_{DS} and I_D for a constant V_{GS}.
5. The drain resistance is found from the graph

$$r_d = \Delta V_{DS} / \Delta I_D$$

Transfer Characteristics:

1. Connections are made as per the circuit diagram.
2. Drain –source voltage V_{DS} is kept constant (say 5v), the gate – source voltage V_{GS} is varied insteps of 1v (-VE voltage) and the corresponding drain current I_D values are tabulated.
3. The above procedure is repeated for V_{DS} = 10v, 15v,
4. Graph is plotted between V_{GS} and I_D for a constant V_{DS}.
5. The trans conductance is found from the graph

$$g_m = \Delta I_D / \Delta V_G$$

REVIEW QUESTIONS:

1. Why it is called by name “field effect transistor”?
2. What are the advantage of FET OVER BJT?
3. What are the disadvantages of FET?
4. What is the significance of arrowhead in FET symbol?
5. Why FET is called unipolar device
6. Define VVR.
7. What are the applications of FET?
8. Why FET is called us voltage controlled device?
9. What are the characteristics of JFET?

RESULT:

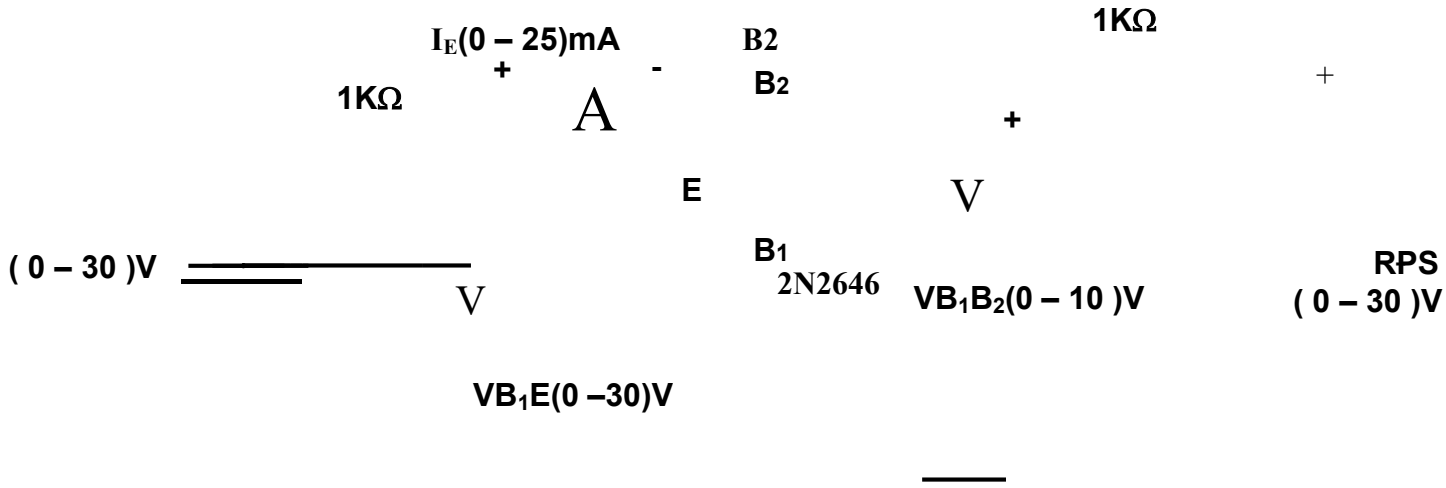
Thus the drain and transfer for characteristics of JFET is drawn.

Drain resistance r_d =

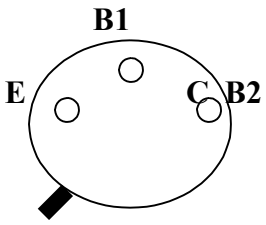
Trans conductance g_m =

Amplification factor =

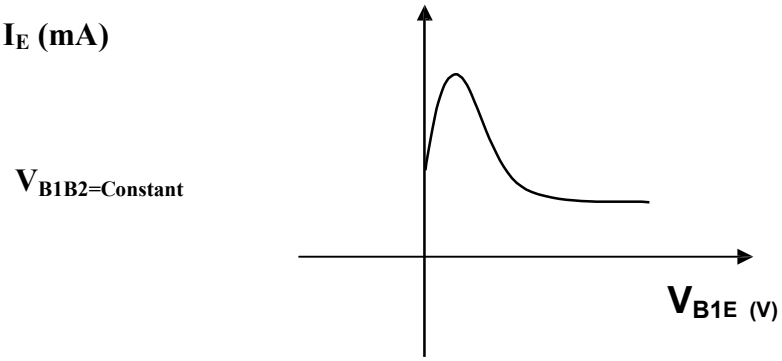
CIRCUIT DIAGRAM:



PIN DIAGRAM



MODEL GRAPH



EX. NO: 4

CHARACTERISTICS OF UJT AND GENERATION OF SAWTOOTH WAVEFORMS

AIM:

To plot VI Characteristics of UJT and to calculate its intrinsic standoff ratio.

APPARATUS REQUIRED:

S.No	Components	Specification	Quantity
1	UJT	(2N2646),	1
2	Resistors	1KΩ	2
3	Ammeter	(0-25) mA	1
4	Voltmeters	(0-10)V	2
5	Regulated dual power supply	(0-30) V	1
6	Bread board & connecting wires.		

THEORY:

Unijunction transistor is a negative resistance silicon controlled device. UJT has three terminals emitter(E), base1(B1)&base2(B2).The UJT finds its main application in switching circuits and in relaxation oscillators. It consists of an n-type Si semiconductor bar, which is lightly doped connected between two ohmic contacts B1 and B2. A heavily doped P-region is diffused into the n-type bar forming a pn junction in the middle of the base bar. A terminal is taken out of this region & named as emitter. The emitter is always forward biased with respect to the base 1 and base 2 is kept at a higher +ve potential with respect to base 1.

INTRINSIC STAND-OFF RATIO:

We know that, from the equivalent circuit,

$$V_{B1} = V_{BB}.R_{b1} = \eta V_{BB}$$

$$R_{B1}+R_{B2}$$

The diode firing takes place when $V_E > (V_{B1}+V_D)$

Where V_D is voltage drop across diode. The emitter firing potential is given by,

$$Vp = \eta V_{BB} + V_D$$

where V_D is 0.7V

$$\eta = \frac{Vp - V_D}{V_{BB}}$$

TABULAR COLUMN:

V_{B1B2} = 2v		V_{B1B2} = 4v		V_{B1B2} = 6v	
V_{B1E}(v)	I_E(mA)	V_{B1E}(v)	I_E(mA)	V_{B1E}(v)	I_E(mA)

PROCEDURE:

1. Connections are given as per the circuit diagram.
2. The voltage across B1and B2 (V_{B1B2}) is kept constant (say 5v), emitter voltage V_{B1E} is varied insteps & the corresponding I_E values are tabulated.
3. The above procedure is repeated for V_{B1B2}=10V.
4. Graph is plotted between V_{B1E} and I_E for a constant value of V_{B1B2}.
5. From the graph, peak voltage & valley voltage is obtained.

REVIEW QUESTIONS:

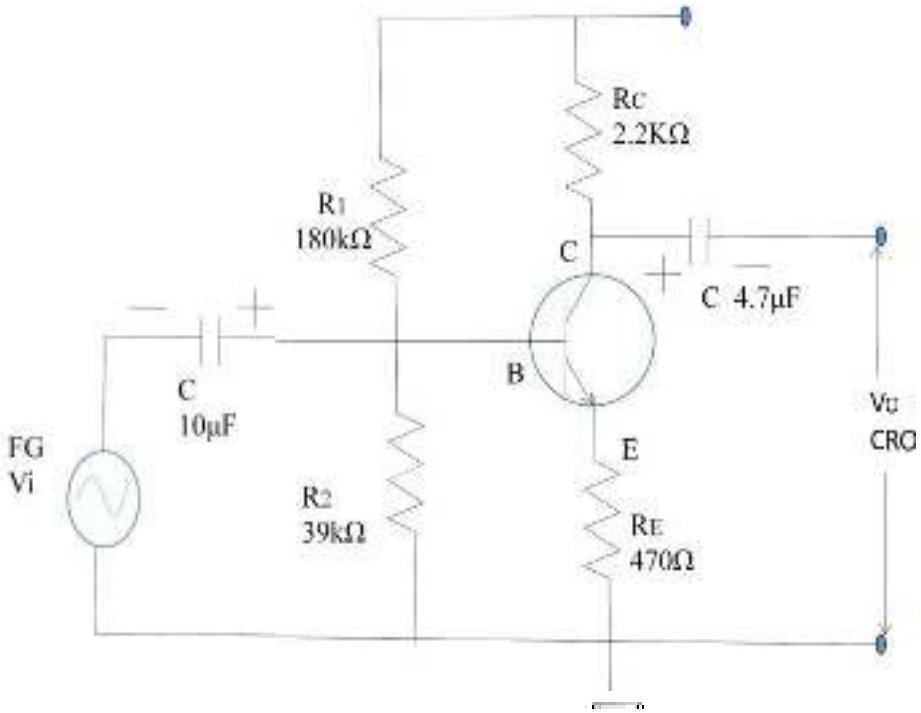
1. What are the applications of UJT?
2. Explain the negative resistance region in case of UJT?
3. What are other names for UJT?
4. What is intrinsic stand off ratio?
5. Define valley voltage & peak voltage?
6. Differentiate BJT and UJT
7. What does UJT stands for? Justify the name UJT.

RESULT:

Thus the static emitter characteristics of UJT drawn & the following values were determined.

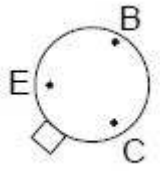
Peak voltage =
Peak current =
Valley voltage =
Valley current =

CIRCUIT DIAGRAM FOR CE AMPLIFIER WITH SELF BIAS:



PIN DIAGRAM:

Bottom view



Symbol

EX NO: 5

DESIGNFREQUENCY RESPONSE CHARACTERISTICS OF A COMMON EMITTER AMPLIFIER

AIM:

To design and construct BJT CE Amplifier using voltage bias (self bias) with and without bypassed emitter resistor.

To measure the gain and to plot the frequency response and to determine the gain bandwidth product.

APPARATUS REQUIRED:

Sl.No	Equipments/Components	Range/Details	Qty
1	RPS	(0-30)V	1
2	Resistors		
3	Capacitors		
4	Transistors	BC107	1
5	CRO	(0-30)MH_Z	1
6	AFO	(0-3) MH_Z	1
7	Bread Board, Connecting Wires		

Take F = 100Hz and h_{ie} = 1.6 KΩ

$C = 1/ (2\pi \times R_i \times F)\ \mu F$

$F = 1/2\pi R_C C_o$

$C_o = 1/ (2\pi \times R_C \times F)\ \mu F$

Calculation:

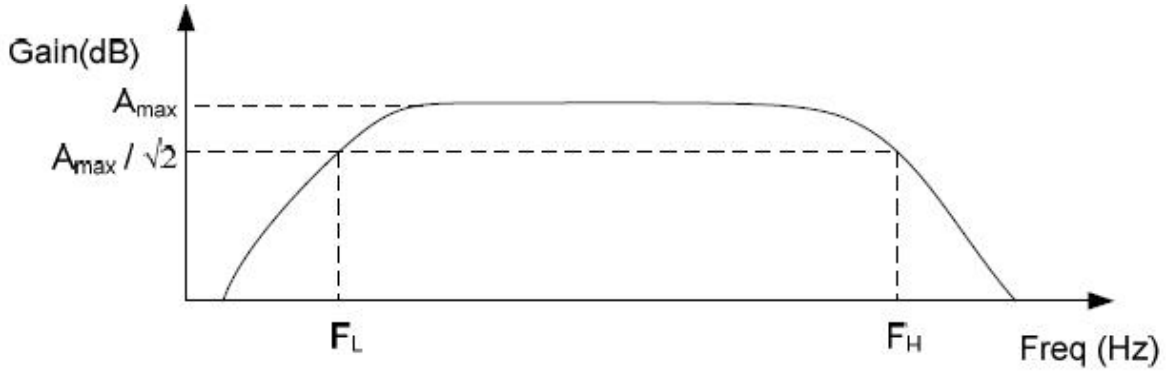
Bandwidth = $f_H - f_L$

TABULATION:

V_i =

Frequency (Hz)	Vo (V)	Gain = Vo / Vi	Gain= 20log(Vo/Vi)dB

MODEL GRAPH:



PROCEDURE:

(1) Connect the circuit as per the circuit diagram

(2) Set V_{in} = 2V in the signal generator. Keeping input voltage constant, vary the frequency from 1Hz to 3MHzin regular steps.

(3) Note down the corresponding output voltage.

(4) Plot the graph: Gain in dB Vs Frequency in Hz.

(5) Calculate the Bandwidth from the Frequency response graph.

DESIGN:

Choose β= 100, V_{CC} = 12V, I_C = 2mA and S≤ 5

Design of R_C and R_E:

By applying KVL to output side,

$V_{CC} = I_C R_C + V_{CE} + I_E R_E$

$V_E = V_{CC}/10$

$V_E = I_E R_E$

$R_E = V_E/I_E$ (since $I_C + I_B = I_E$ and $I_B = I_C/\beta$)

$V_{CE} = V_{CC}/2$

$R_C = 0.4V_{CC}/I_C$

Design of R_1 and R_2:

V_{BE} = 0.7V

$$S = \frac{(1+\beta)}{1+\beta}$$

$V_{TH} = I_B R_{TH} + V_{BE} + (I_B + I_C)R_E$

$R_1 = R_{TH}V_{CC}/V_{TH}$

$R_2 = R_1 V_{TH}/(V_{CC} - V_{TH})$

Design of Capacitor:

$R_i = R_B \parallel h_{ie}$

$F = 1/2\pi R_i C$

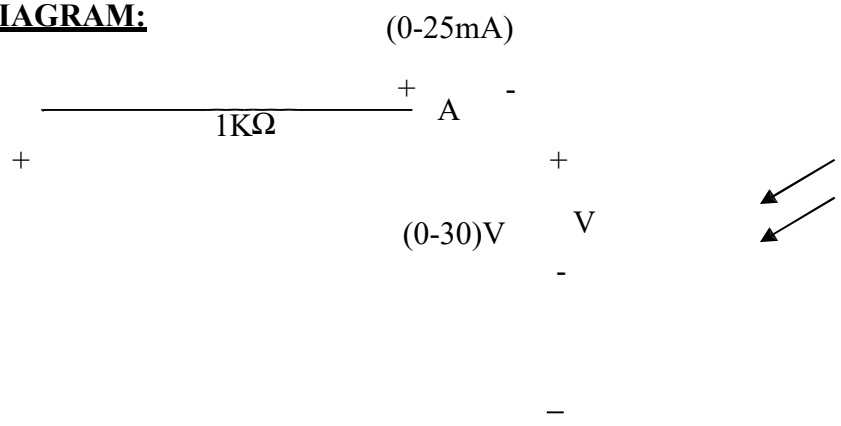
REVIEW QUESTIONS:

1. What are the operating modes of BJT with reference to junction biasing?
2. Why CE configuration is preferred over CB configuration?
3. Write some applications of CE amplifier?
4. What will be the input and output impedance of CE amplifier?
5. What is the voltage and current gain of CE amplifer?

RESULT:

Thus a BJT CE Amplifier with self bias is designed and implemented and the frequency response curve is plotted.

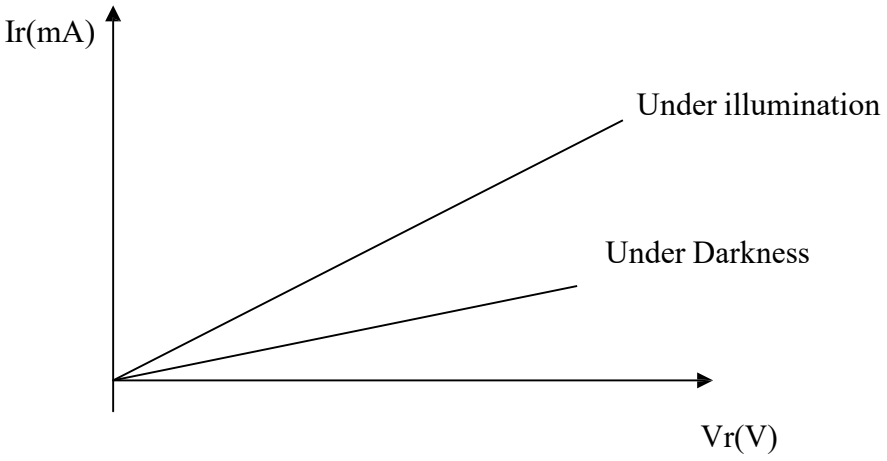
CIRCUIT DIAGRAM:



TABULATION:

Reverse voltage (V)	Reverse current (In darkness) (mA)	Reverse current (In illumination) (mA)

MODEL GRAPH:



EX NO: 6(a)

CHARACTERISTICS OF PHOTODIODE

AIM:

To study the characteristics' of a photodiode.

APPARATUS REQUIRED:

S.No	Component	Range/Specification	Quantity
1	Photodiode		1
2	Resistor	1KΩ	1
3	Ammeter	0-25mA	1
4	Voltmeter	0-30 V	1
5	RPS	0-30 V	1
6	Breadboard and connecting wires		

THEORY:

Photodiode is connected in reverse biased condition. The depletion region width is large under normal condition. It carries small reverse current. When light is incident through glass window on PN junction, photons in the light bombards with the PN junction and some energy is imparted to the valence electron. Due to this valence electrons are dislodged from the covalent bonds and become a free electron. Thus total number of minority carriers' increases thereby increasing the reverse current.

PROCEDURE:

1. Switch on the power supply.
2. Photodiode is subjected to darkness and illumination and the following steps are followed each time.
3. By varying the supply voltage in steps of 1V, note ddown the reverse voltage(V_r) and corresponding reverse current (I_r)
4. Plot the graph between reverse voltage and reverse current.

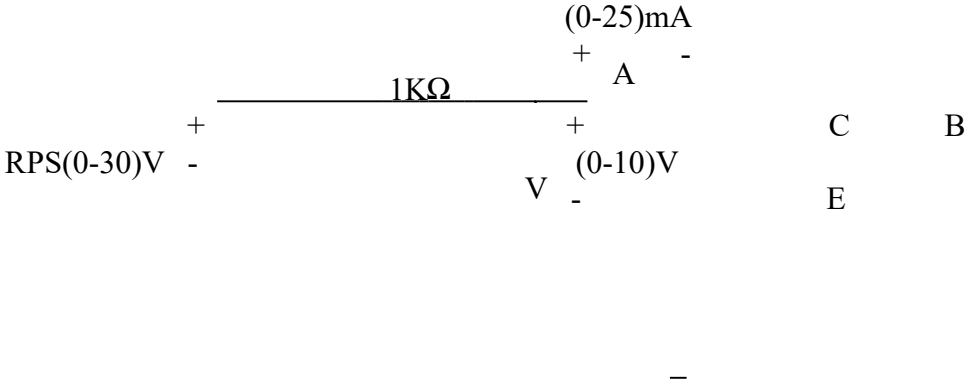
REVIEW QUESTIONS:

1. Explain the operation of a photodiode.
2. Applications of a Photodiode.
3. What is photodiode?
4. Why is a photodiode reverse biased?
5. What is the output signal of a photodiode?
6. What happens if the photodiode is biased with a voltage larger than the specified maximum reversebias?
7. What is Photo voltaic effect?

RESULT:

Thus the characteristic of a photodiode was studied.

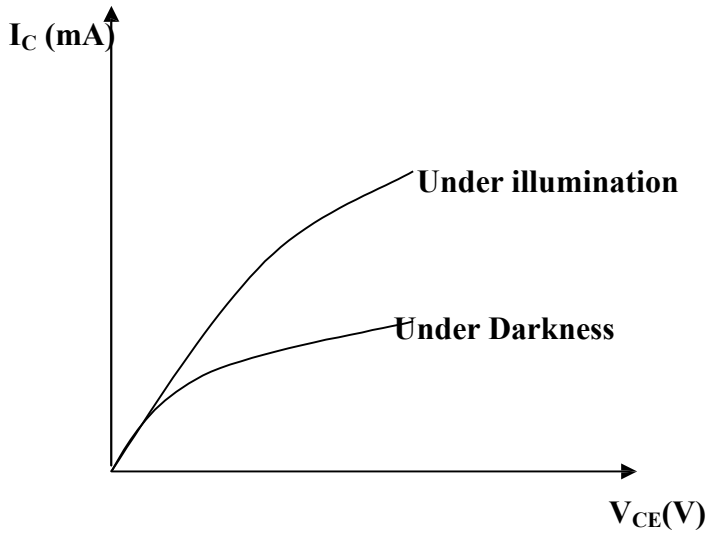
CIRCUIT DIAGRAM:



TABULATION:

S.No	Under Darkness		Under illumination	
	V_{CE}(V)	Ic(mA)	V_{CE}(V)	I_c(mA)

MODEL GRAPH:



EX NO: 6(b)

CHARACTERISTICS OF PHOTOTRANSISTOR

AIM:

To study the characteristics of a phototransistor.

APPARATUS REQUIRED:

S.No	Component	Range/Specification	Quantity
1	Phototransistor		1
2	Resistor	1KΩ	1
3	Ammeter	0-25mA	1
4	Voltmeter	0-10 V	1
5	RPS	0-30 V	1
6	Breadboard and connecting wires		

THEORY:

Phototransistor helps us to achieve photo multiplication or photo current enhancement. In phototransistor, pairs are generated on the base region by illumination and some majority carriers diffuse into the emitter, resulting in an injection current which is large. The base load can even be left open but still majority current will cause injection in this structure.

PROCEDURE:

1. Switch on the power supply.
2. Photodiode is subjected to darkness and illumination and the following steps are followed each time.
3. By varying the supply voltage in steps of 1V, note down the voltage(V_{CE}) and corresponding current (I_c)
4. Plot the graph between voltage and current.

REVIEW QUESTIONS:

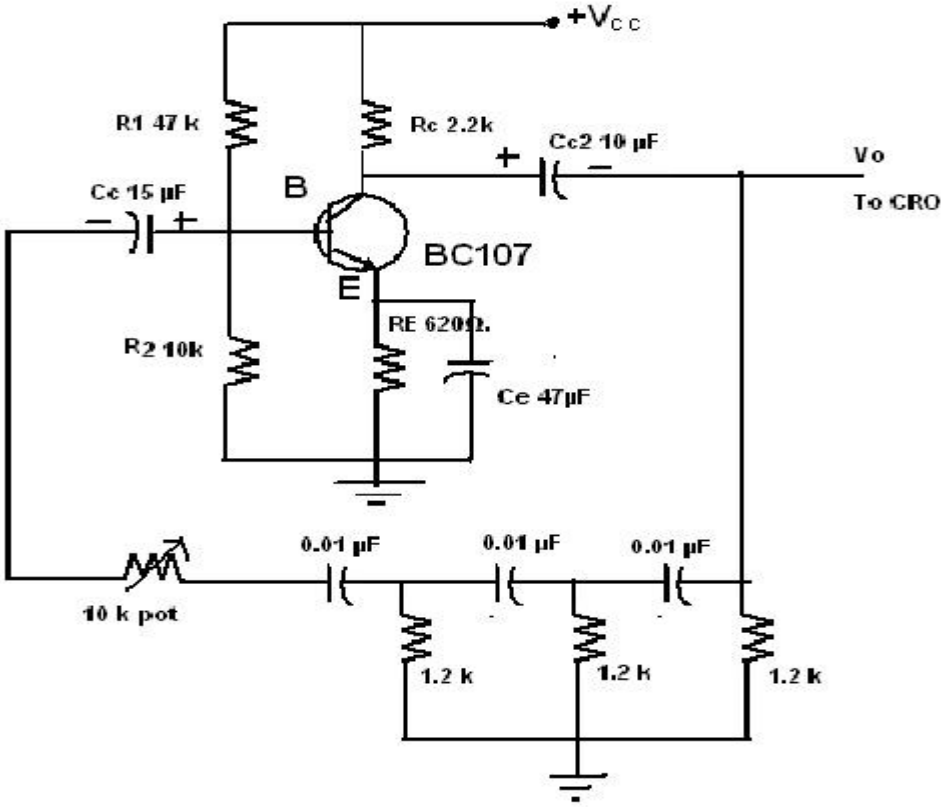
1. Explain the operation of a phototransistor.
2. Explain photo multiplication effect**.**
3. What is a Phototransistor?
4. What are the applications of phototransistor?
5. What are the features of Phototransistor?
6. What are the advantages and disadvantages of Phototransistor?
7. Difference between Photodiode and Phototransisitor.

RESULT:

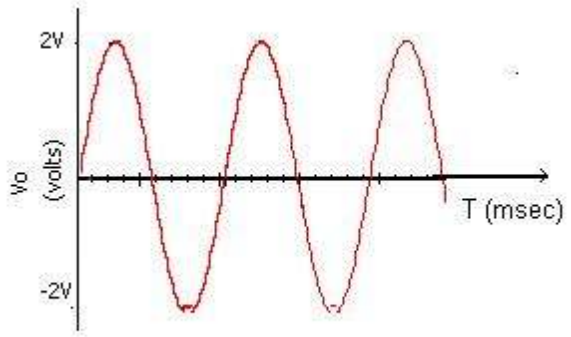
Thus the characteristic of a phototransistor was studied.

CIRCUIT DIAGRAM

RC PHASE SHIFT OSCILLATOR



MODEL GRAPH



EX NO: 7(a)

RC PHASE SHIFT OSCILLATOR

AIM:

To design and construct a RC phase shift oscillator for the given frequency (f0).

APPARATUS REQUIRED:

S.NO	ITEM	RANGE	Q.TY
1	TRANSISTOR	BC 107	1
2	RESISTOR		
3	CAPACITOR		
4	CRO	(0 – 30) MHz	1
5	RPS	(0-30) V	1
6	FUNCTION GENERATOR	(0-1)MHz	1

THEORY:

In the RC phase shift oscillator, the required phase shift of 180˚ in the feedback loop from the output to input is obtained by using R and C components, instead of tank circuit. Here a common emitter amplifier is used in forward path followed by three sections of RC phase network in the reverse path with the output of the last section being returned to the input of the amplifier. The phase shift Φ is given by each RC section $\Phi=\tan^{-1}(1/\omega RC)$. In practice R -value is adjusted such that Φ becomes 60˚. If the value of R and C are chosen such that the given frequency for the phase shift of each RC section is 60˚. Therefore at a specific frequency the total phase shift from base to transistor's around circuit and back to base is exactly 360˚ or 0˚. Thus the Barkhausen criterion for oscillation is satisfied.

DESIGN:

Vcc=12v, Ic=1mA, β=100,RE = 560 Ω

Vce=Vcc/2=6V, Vre=0.1Vcc=1.2V

Vb=Vre+0.7=1.9V,

R1=Vcc/10Ib – R2

=12/(10*20μA) – 10 K =47 K Ω

R2=Vb/10Ib = .9/(10*20μA)=9.5K Ω=10 K Ω

Rc=Vcc-Vce-(IeRe/Ic)

=2.4 K Ω =2.2 KΩ

$Fo=1/(2\pi R \sqrt{(6+4(Rc/R))})$

$C=1/2\pi Rc\sqrt{(6+4(Rc/R))}$

$=1/(6.28*10*10^3*4 \sqrt{(6+4(2.2*10^3/10))})$

$=0.0015\ \mu F$

PROCEDURE:

1. The circuit is constructed as per the given circuit diagram.
2. The supply voltage of +12 volts and ground are given to the constructed circuit.
3. The output sine wave generated from the circuit is verified in the CRO and the theoretical frequency is calculated and verified with the practical frequency.

REVIEW QUESTIONS

1. What are the conditions for sustained oscillator
2. What is Barkhausen criterion?
3. What are the classifications of Oscillators?
4. What is the advantage and disadvantage of negative feedback?
5. What is oscillator phase shift circuit?
6. What type of feedback is preferred in oscillators?
7. How does oscillation start in oscillators?
8. What is the frequency of RC phase shift oscillator?
9. Why RC oscillators cannot generate high frequency oscillations?
10. What are the applications of RC phase shift oscillators?
11. What phase shift does RC phase shift oscillator produce?
12. Why we need a phase shift between input and output signal?
13. How is phase angle determined in RC phase shift oscillator?

RESULT :

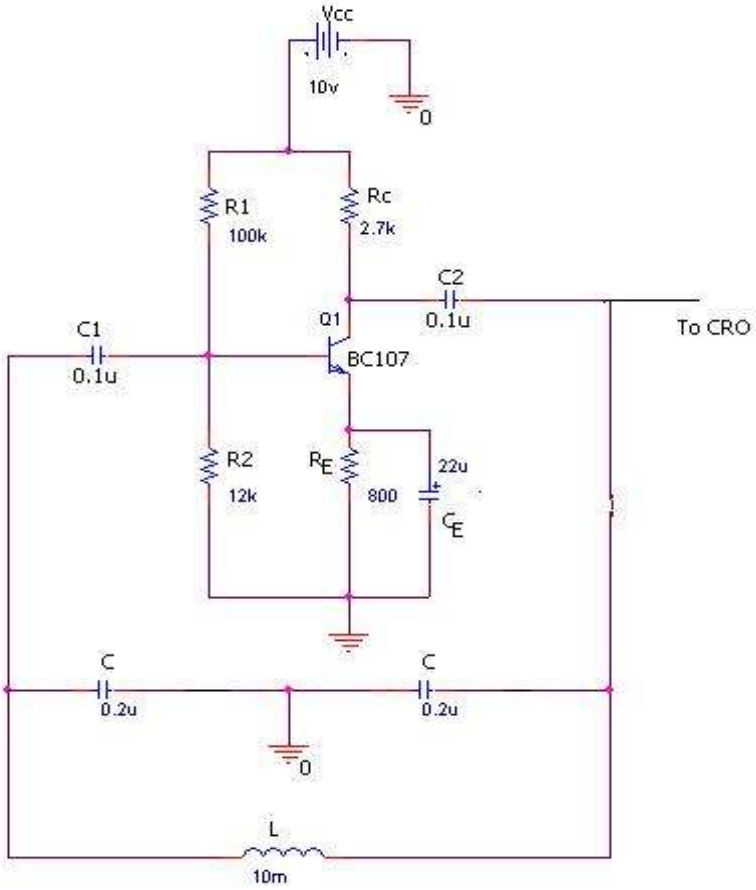
Thus a sine wave with required phase shift is produced using transistor phase shift oscillator. Thus,

Theoretical Oscillation Frequency = _____

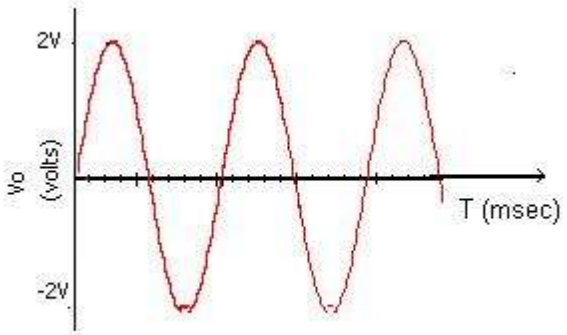
Practical Oscillation Frequency = _____

CIRCUIT DIAGRAM

COLPITTS OSCILLATOR



MODEL GRAPH



EX NO: 7(b)

COLPITTS OSCILLATOR

AIM :

To design and construct a Hartley and Colpitts oscillator.

COMPONENTS AND EQUIPMENTS REQUIRED:

S.No.	Components/Equipments	Specifications	Quantity
1	Transistor	BC 107	1
2	Resistor	100kΩ,3.9kΩ,12kΩ,800Ω	Each 1
3	Capacitor	0.1μF	2
4	Decade Capacitance box		2
5	Decade Inductance box		2
6	CRO	(0-30)MHz	1
7	RPS	(0-30) V	1

DESIGN:

Vcc =10V, I_C =1.2mA, R_B =15k Ω

$V_E = Vcc /10 = 10V /10 = 1V$

$I_E \approx Ic = 1.2mA$

$V_E = I_E R_E$

$R_E = V_E / I_E = 1V / 1.2mA$

$R_E = 833.33\Omega$

Choose , $R_E = 800\ \Omega$

$Vcc = IcR_C + V_{CE} + V_E$

$Rc = (Vcc – V_{CE} – V_E) / Ic = (10 – 5 – 1) / 1.2mA$

$Rc = 3.3k\Omega$

Choose , $Rc = 3.9k\Omega$

$V_{BE} = V_B – V_E$

$V_B = V_{BE} + V_E = 0.7 + 1 = 1.7\ V$

$V_B = (Vcc * R2)/ (R1+R2) = 15k\Omega$

$R2/(R1+R2) = 1.7 /10 = 0.17$

$R1 = 15k\Omega / 0.17 = 88.24k\Omega$

Choose , $R1 = 100k\Omega$

$R2/(R1+R2) = 0.17$

$R2 = 18k\Omega$

Choose , R2 =12kΩ
Let C1 =C2 = 0.1μF

THEORY:

If gain A of the amplifier is just sufficient to over come the attenuator β of the β - network. We get sinusoidal oscillations. Mathematically If Aβ is for greater than 1 square wave results in however, if Aβ is less than 1 no oscillations will occur. The Colpitts and Hartley Oscillator is a LC oscillator. Generally, LC oscillators are designed to operate in the radio – frequency range above 1MHz however, they can also be designed to produce oscillations in the low audio – frequency range. But for low frequency operation, the size of the inductors to be used become larger and larger as the frequency becomes smaller and smaller and this puts a limit on the low frequency range of oscillators employing LC – coupling network.

PROCEDURE :

1. Connect the circuit as per the circuit diagram.
2. For the Colpitts oscillator adjust the capacitance in the tank circuit to get a sinusoidal signal of desired frequency
3. Plot the output obtained in the linear graph.

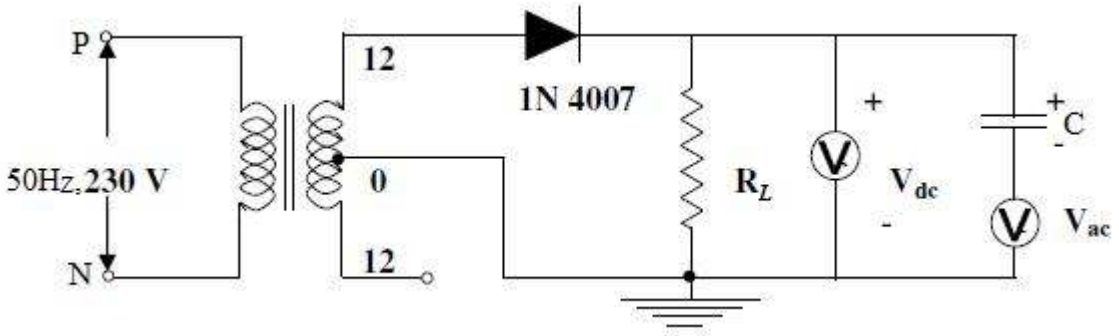
REVIEW QUESTIONS:

1. Which oscillator is very suitable for radio frequency range applications?
2. What is the difference between Hartley and Colpitts oscillators in construction?
3. Why are Colpitts oscillators used to generate fixed radio-frequency signals?
4. What is the frequency of Hartley and Colpitts oscillator?
5. What are the advantages and disadvantages of Hartley and colpitts oscillator?
6. Name two high frequency Oscillators.
7. What are the essential parts of an Oscillator

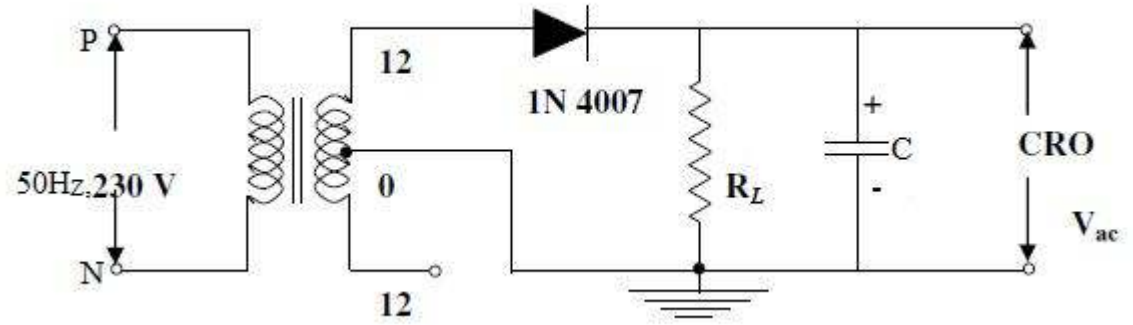
RESULT:

Thus Colpitts oscillator is designed and constructed, and the output sine wave form is observed. Then practical oscillation frequency is calculated & compared with theoretical oscillation frequency.

CIRCUIT DIAGRAM FOR HALF WAVE RECTIFIER WITHOUT FILTER:



CIRCUIT DIAGRAM FOR HALF WAVE RECTIFIER WITH FILTER:



EX NO:8(a)

HALF WAVE RECTIFIER

AIM:

To design a half wave rectifier with simple capacitor filter.

To measure the DC voltage under load and ripple factor and to compare with calculated values.

APPARATUS REQUIRED:

Sl.No	Equipments/Components	Range/Details	Qty
1	Multimeter		1
2	Resistors		
3	Capacitors		
4	Diode	1N4001	1
5	CRO	(0-30)MH_Z	1
6	Transformer	230V/(9-0-9) V	1
7	Bread Board, Connecting Wires		

PROCEDURE:

Without Capacitor:

(1) Test your transformer: Give 230V, 50Hz source to the primary coil of the transformer and observe the AC waveform of rated value without any distortion at the secondary of the transformer.

(2) Connect the half wave rectifier as shown in figure.

(3) Measure the V_{dc}& V_{ac} using DC and AC Voltmeters.

(4) Calculate the ripple factor $r = V_{ac} / V_{dc}$

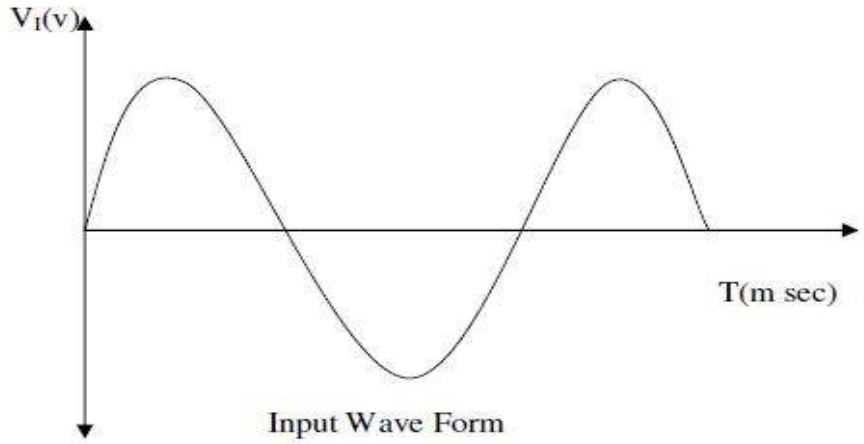
(5) Compare the theoretical ripple factor with the practical ripple factor.

With capacitor:

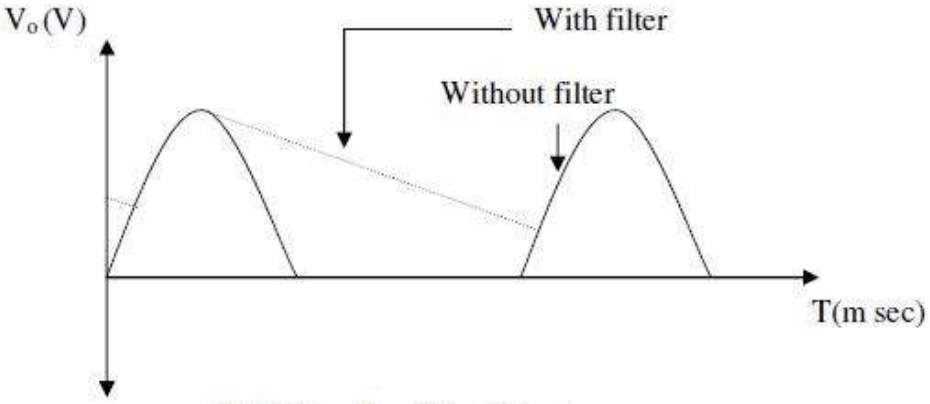
(6) Connect the half wave rectifier with filter circuit as shown in fig.

(7) Connect CRO across load.

MODEL GRAPH:



Input Wave Form



Half Wave Rectifier Output

(8) Keep the CRO switch in ground mode and observe the horizontal line and adjust it to the X-axis.

(9) Switch the CRO into DC mode and observe the waveform.

Calculations:

Without Filter:

R_F = Forward resistance of diode =30Ω

R_L = Load resistance

$$= \frac{}{(+)}$$

$$= \frac{}{( )}$$

Ripple factor =

$$= (-)$$

Average load voltage at no load (V_{NL}) = V_m/π

Average load voltage at full load =

$$= 2(+)$$

With Filter:

f = 50H_Z

$$= +$$

$$= \left(\frac{1}{2\sqrt{3}}\right)(+)$$

Ripple factor = r = V_{rms} / V_{dc}

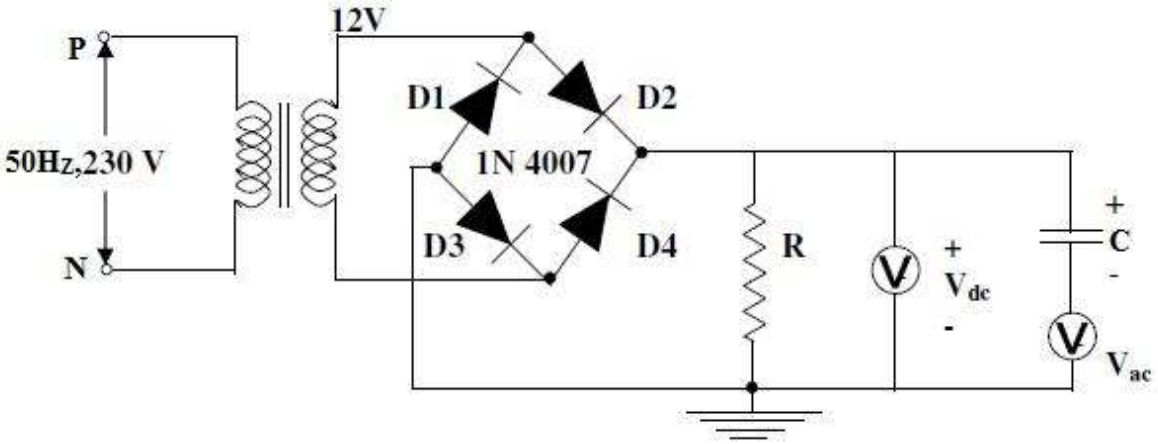
REVIEW QUESTIONS

1. What is a rectifier?
2. What is ripple factor(Y)?
3. List the types of Rectifiers
4. Compare the various types of Rectifiers
5. What is efficiency?
6. What is PIV?
7. What are the applications of rectifier?
8. What are advantages and disadvantages of half-wave rectifier?

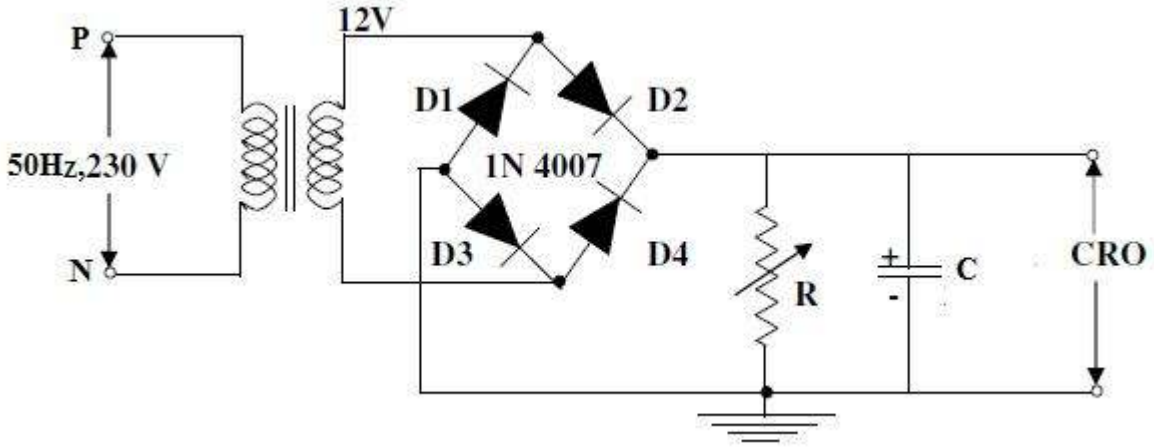
RESULT:

Thus the half wave rectifier is designed with and without capacitor filter and the corresponding dc output voltages and the ripple factors are measured and verified with the theoretical values.

CIRCUIT DIAGRAM FOR FULL WAVE RECTIFIER WITHOUT FILTER:



CIRCUIT DIAGRAM FOR FULL WAVE RECTIFIER WITH FILTER:



EXP.NO: **8(b)**

FULL WAVE RECTIFIER

AIM:

To design a Full wave rectifier with and without simple capacitor filter.

To measure the DC voltage under load and ripple factor and to compare with calculated values.

APPARATUS REQUIRED:

Sl.No	Equipments/Components	Range/Details	Qty
1	Multimeter		1
2	Resistors		
3	Capacitors		
4	Diode	1N4001	4
5	CRO	(0-30)MH_Z	1
6	Transformer	250V/ (9-0-9)V	1
7	Bread Board, Connecting Wires		

PROCEDURE:

Without Capacitor

(1) Test your transformer: Give 230v, 50Hz source to the primary coil of the transformer and observe the AC waveform of rated value without any distortion at the secondary ofthe transformer.

(2) Connect the full wave rectifier as shown in figure.

(3) Measure the Vdc & Vac using DC and AC Voltmeters.

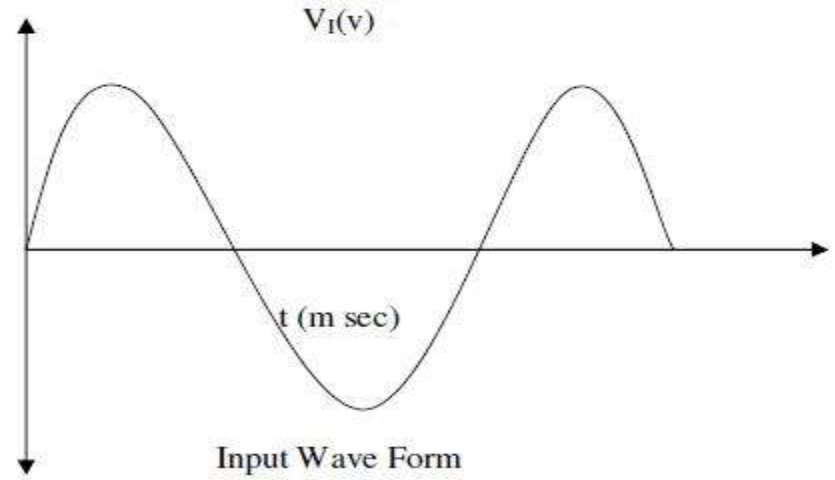
(4) Calculate the Ripple factor r = Vac / Vdc

(5) Compare the theoretical ripple factor with the practical ripple factor.

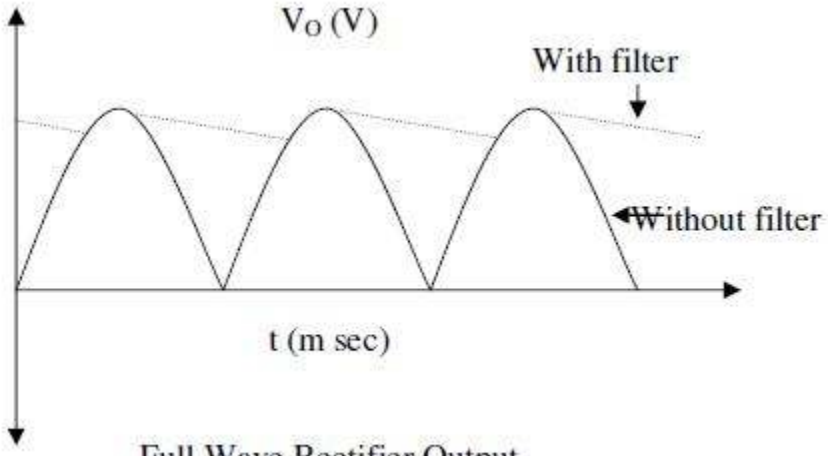
With capacitor:

(6) To plot ripple peak-to-peak voltage Vs.

MODEL GRAPH:



Input Wave Form



Full Wave Rectifier Output

(7) To get a variable load resistance a number of 500Ω resistances connected in parallel.

(8) Plot the graph I_{dc} Vs ripple peak to peak.

(9) The above steps are repeated for the various values of capacitance.

Calculations:

Without Filter:

R_F = Forward resistance of diode =30Ω

R_L = Load resistance

$$= \frac{2}{}$$

$$= \sqrt{}$$

Ripple factor =

$$= -$$

Average load voltage at no load (V_{NL}) = $2V_m/\pi$

Average load voltage at full load =

$$= \frac{2}{(2 +)}$$

With Filter:

f = 50H_Z

$$= + $$

$$= \left(\frac{1}{4\sqrt{3}}\right)(+)$$

Ripple factor = r = V_{rms} / V_{dc}

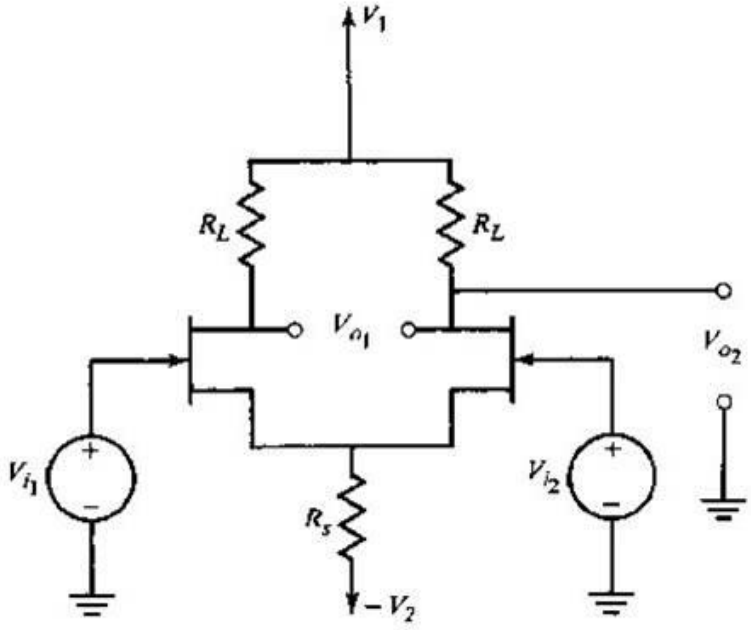
REVIEW QUESTIONS

1. Define Full wave Rectifier
2. What are the merits of Full Wave Rectifier
3. What is the major disadvantages of Full Wave Rectifier
4. What is the efficiency of bridge rectifier?
5. In filters capacitor is always connected in parallel, why?
6. If the output voltage of a bridge rectifier is 100V, the PIV of diode will be
7. What are the differences between Half-wave and Full-wave rectifier?

RESULT:

Thus the Full wave rectifier is designed with and without capacitor filter and the corresponding dc output voltages and the ripple factors are measured and verified with the theoretical values.

CIRCUIT DIAGRAM:



MODEL CALCULATIONS:

i) For common mode signal:
Gain Ac = Vo / Vi
Ac =
ii) For differential mode signal:
Gain Ad = Vo / Vi
Ad =
CMRR = 20 log (Ad / Ac).

EX.NO:9

DIFFERENTIAL AMPLIFIERS USING FET

AIM:

To construct the Differential Amplifier in Differential mode and to find the common moderejection ratio (CMRR).

APPARATUS REQUIRED:

Sl.No	Equipments/Components	Range/Details	Qty
1	FET		2
2	Resistors		
3	RPS		2
4	Capacitors		
5	CRO	(0-30)MH_Z	1
6	Bread Board, Connecting Wires		

THEORY:

A differential amplifier is a type of electronic amplifier that amplifies the difference between two input voltages but suppresses any voltage common to the two inputs. Differential amplifiers are usually implemented with a basic two-transistor circuit called a long-tailed pair or differential pair. This circuit was originally implemented using a pair of vacuum tubes. The circuit works the same way for all three-terminal devices with current gain. The long-tail resistor circuit bias points are largely determined by Ohm's Law and less so by active component characteristics.

FORMULA:

C.M.R.R = | Ad/Ac |
C.M.R.R in dB = 20 log | Ad/Ac |
Ad = Differential mode gain
Ac = Common mode gain

PROCEDURE:

1. Connections are made as per the circuit diagram.
2. Switch ON the RPS
3. Vary the input voltages using function generator and note the corresponding output voltage.
4. Reduce the RPS voltage to 0 V
5. Calculate the Gain.
6. Calculate the CMRR

REVIEW QUESTIONS:

1. What is Differential amplifier?
2. What is difference between amplifier and Diff.amplifier?
3. Sketch the circuit diagram of Diff amplifier using BJT.
4. List out the ap[placation of Differential amplifier.
5. What is the mode of operations in Diff.Amp?
6. What is CMRR?
7. What is the use of CMRR?
8. What is gain?
9. What is the unit of current and voltage gain?
10. Compare the application of Diff.amp using FET with Diff.Amp using BJT.

RESULT:

Thus the differential amplifier is constructed and CMRR has been calculated.

EX. NO: 10

STUDY OF CRO FOR FREQUENCY AND PHASE MEASUREMENTS

AIM:

To Study the operation of CRO and measure frequency and phase.

APPARATUS REQUIRED:

Sl.No	Equipments/Components	Range/Details	Qty

FORMULA:

Amplitude = No. of vertical divisions * Volts/div.
Time period = No. of horizontal divisions * Time/div.
Frequency=(1/T)Hz

PROCEDURE:

1. Connect the Function generator with CRO.
2. Switch ON the CRO and Function generator
3. Set the given frequency in function generator.
4. Observe the frequency and phase angle in CRO
5. Reduce the frequency to 0 Hz
6. Switch OFF the Function generator and CRO

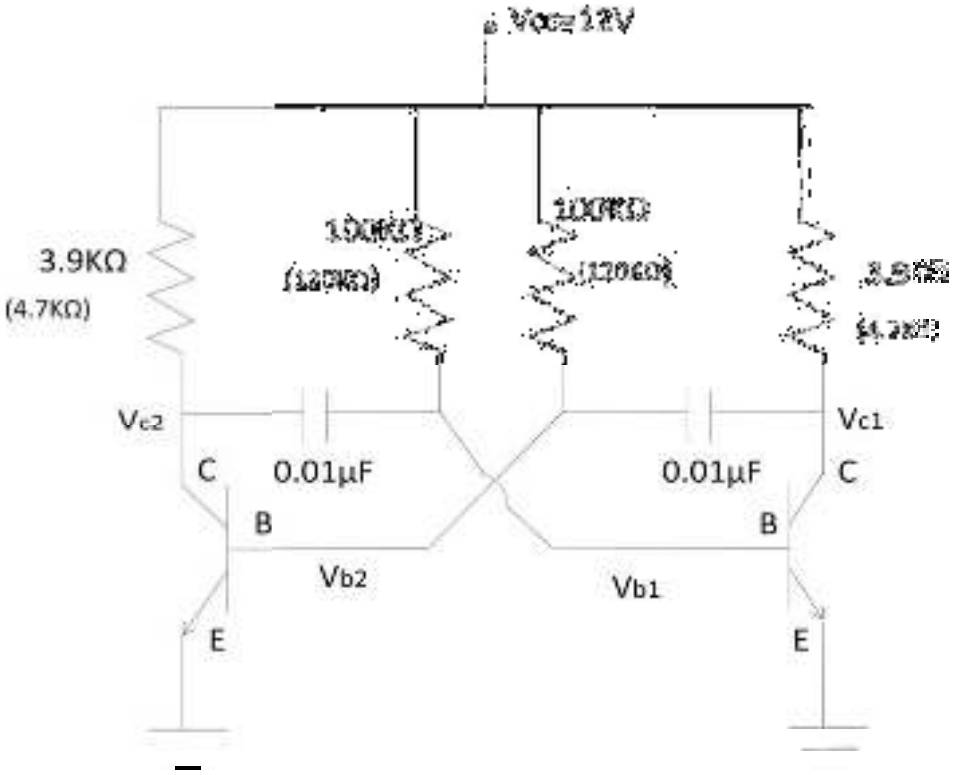
REVIEW QUESTIONS:

1. What is the use of CRO?
2. Can you name the Manufacture of CRO
3. Explain the working CRO
4. How do you measure the frequency and phase angle in CRO?
5. What is the use of Volt/Div and Time/Div knob in CRO?
6. What is offset error?
7. The measured voltage of CRO is _____
8. What is peak value and peak to peak value?
9. How do you set the external signal to CRO?
10. What is the use of probe and give its specification?

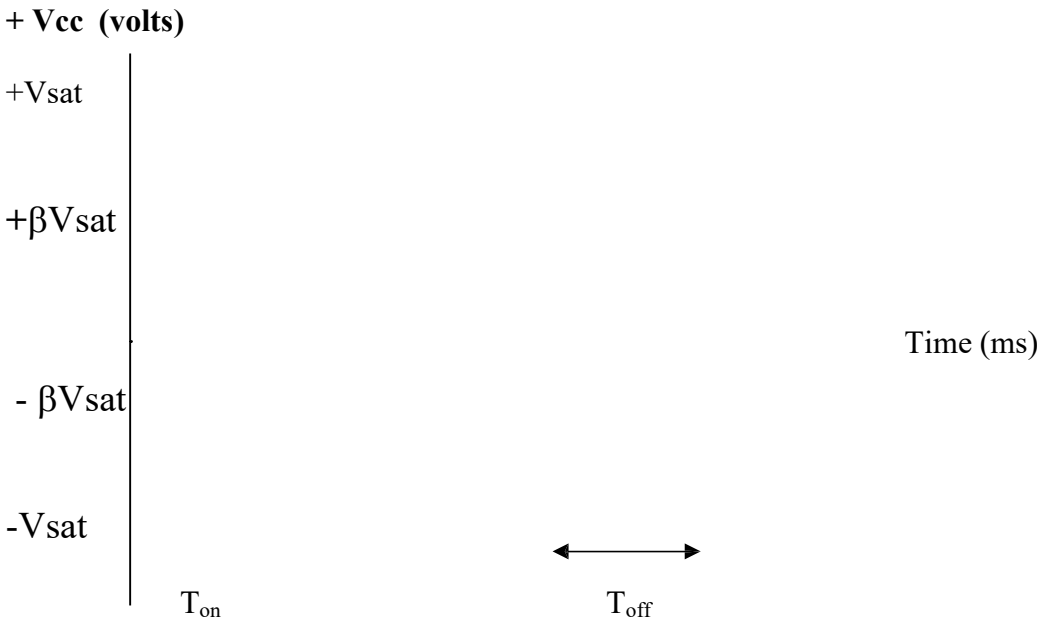
RESULT:

Thus the operation of CRO has been studied and the frequency and phase has been measured.

CIRCUIT DIAGRAM:
Astable Multivibrator



MODEL GRAPH:



EX.NO.11(a):

ASTABLE MULTIVIBRATOR

AIM:

To design an astable multivibrator using transistor to generate a signal of frequency 1kHz.

DESCRIPTION:

ASTABLE MULTIVIBRATOR

Input : Generator does not require input

Output: 1.Output is observed at pin number 6 the output is Square wave at 1KHz and magnitude is ±Vsat

2. At pin no.2 ie across the capacitor it is a charging and discharging voltage (triangular wave) with the magnitude of ±βVsat

APPARATUS REQUIRED :

S.NO	ITEM	RANGE	Q.TY
1	OP-AMP	IC741	1
2	Resistors	5KΩ,1.8KΩ2.2KΩ	1
3	Capacitor	0.1μF	1
4	CRO		1
5	RPS	DUAL(0-30) V	1

DESIGN:

ASTABLE MULTIVIBRATOR

For square waveform generation R1 =1.16R2

Then , freqency of operation f = 1/2RC

Let R2 = 1kΩ , R1=1.16kΩ ≈1.2kΩ

f = 1/2RC = 1kHz

Assuming C = 0.1 uF, R = 1/2fC

Then R = 5K, choose 4.7kΩ

TABULATION :

Astable Multivibrator:

OUTPUT V_O		CAPACITOR VOLTAGE V_C	
Amplitude (volts)	**Time (ms)**	**Amplitude (volts)**	**Time (ms)**

PROCEDURE:

ASTABLE MULTIVIBRATOR

1. The connection is given as per the circuit diagram.
2. Connect the CRO in the output (pin no. 6) and trace the square waveform.
3. Measure the voltage across the capacitor in pin no.2
4. Calculate the practical frequency and compare it with the theoretical frequency.
5. Plot the waveform obtained and mark the frequency and time period.

THEORY:

ASTABLE MULTIVIBRATOR

A simple op-Amp square wave generator is also called as free running oscillator, the principle of generation of square wave output is to force an op-amp to operate in the saturation region. A fraction β=R2/ (R1+R2) of the output is fed back to the (+) input terminal. The output is also fed to the (-) terminal after integrating by means of a low pass RC combination.In astable multivibrator both the states are quasistables. The frequency is determined by the time taken by the capacitor to charge from- βVsat to+βVsat.

REVIEW QUESTIONS:

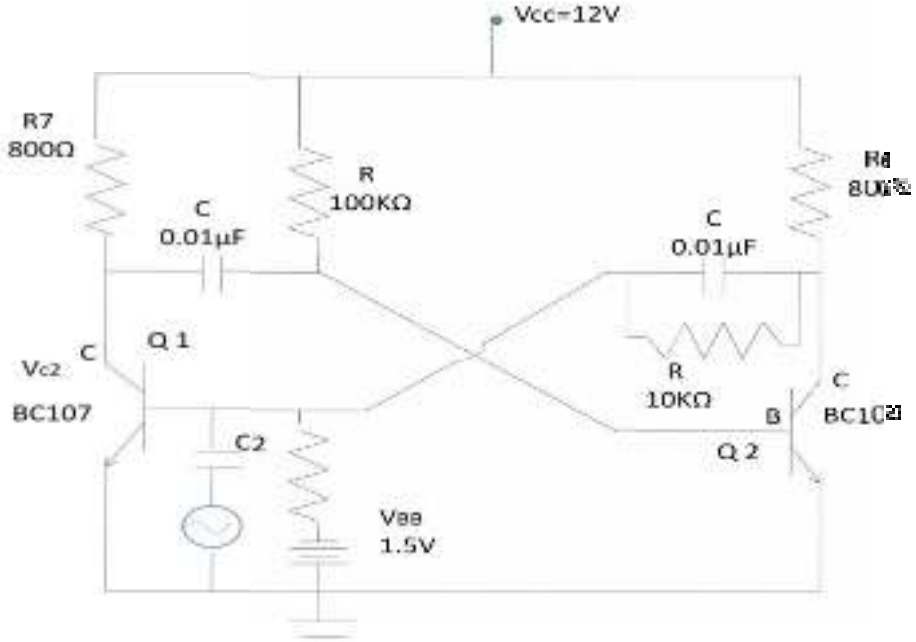
1. What is an op-amp? Why it is called so?
2. List the ideal characteristics of an op-amp.
3. What are the building blocks of an op-amp?
4. Define multivibrator.
5. List the types of multivibrators
6. What is an astable multivibrator?
7. Why astable multivibrator is called as a free running oscillator?
8. State the applications of an astable multivibrator.
9. What is the other name of astable multivibrator?
10. Why astable multi vibrator is called voltage to frequency converter?

RESULT:

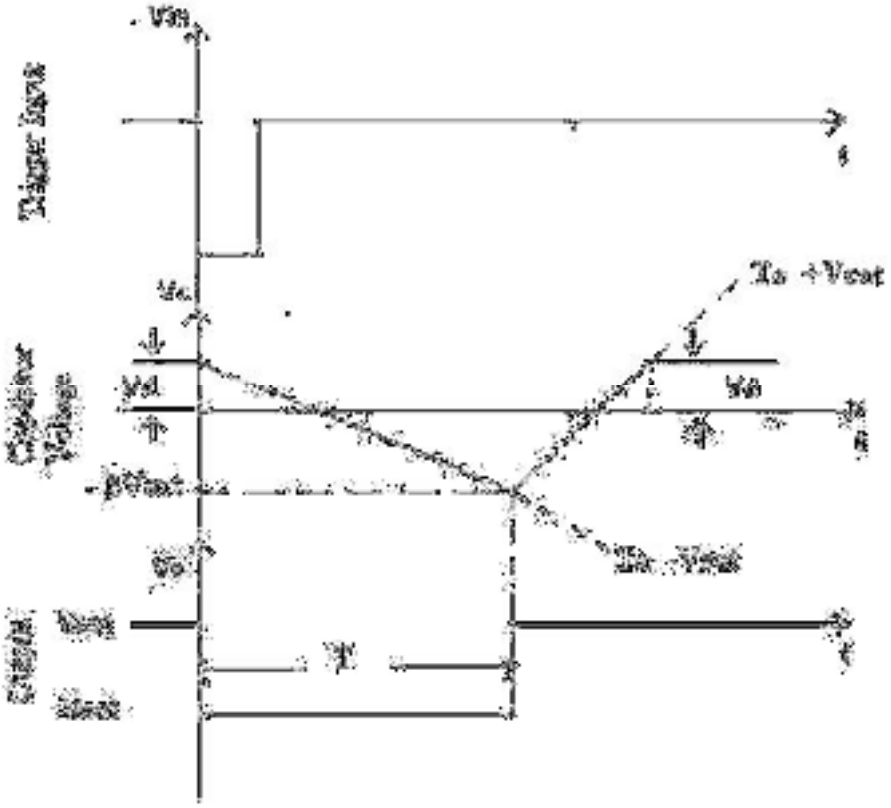
Thus the square waveform is generated using an astable multivibrator .
Theoretical frequency :
Practical frequency :

CIRCUIT DIAGRAM

Monostable Multivibrator:



MODEL GRAPH:



EX.NO.11(b)

MONOSTABLE MULTIVIBRATOR

AIM:

To design a monostable multivibrator using transistors to generate a signal of pulse width.

DESCRIPTION:

MONOSTABLE MULTIVIBRATOR

Input : Apply the trigger input of 1kHz through a RC filter.
Output : Output is obtained at pin no. 6 the pulsewidth of time period 1ms and magnitude is -Vsat. At pin no.2 (i.e.)the voltage across the capacitor is measured in correspondence to the output waveform.

APPARATUS REQUIRED :

MONOSTABLE MULTIVIBRATOR

S.NO	ITEM	RANGE	Q.TY
1	OP-AMP	IC741	1
2	Resistors	15KΩ,1KΩ,1.2KΩ	1,2,1
3	Capacitor	0.1μF	2
4	CRO		1
5	Diode	IN4001	2
6	RPS	DUAL(0-30) V	1

DESIGN:

Given T=1ms and β=0.5

β = R2/(R1+R2)=0.5 then R1 = R2

Let R1=R2 =1KΩ

Pulse width T = 0.69RC

Assume C = 0.1uF

Then R = T/ (0.69 C)

R = 15 kΩ

PROCEDURE:

Monostable multivibrator

1. Connections are given as per the diagram.
2. Input trigger is given to the combination of R4 and C4.
3. Measure the pulse width of the output obtained at pin number 6.
4. Measure the output across capacitor C at pin no.2
5. Compare the observed pulse width T with the theoretical time period.

.

OBSERVATION :

Input trigger :

Amplitude =

T_{ON} = T_{OFF} =

OUTPUT V_O		**CAPACITOR VOLTAGE V_C**	
Amplitude (volts)	**Time (ms)**	**Amplitude (volts)**	**Time (ms)**

5. Plot the input, capacitor and the output waveform in a linear graph sheet

THEORY:

Monostable Multivibrator:

A monostable multivibrator is a timing circuit that changes state once triggered, but returns to its original state after a certain time delay. It has one stable state and the other is quasi stable state hence is also known as a 'one-shot' multivibrator. A negative trigger pulse at the input forces the output of the op amp to logic 'high'. This charges up C which keeps the non-inverting input of the op amp temporarily higher than the inverting input, maintaining the output high for a certain period of time. Eventually C discharges to ground and the op amp output swings back to logic 'low'. The duration of the pulse is defined by R and C. The 'one-shot' has several applications, which include dividing the frequency of the input signal and converting an irregular input pulse to a uniform output pulse.

REVIEW QUESTIONS:

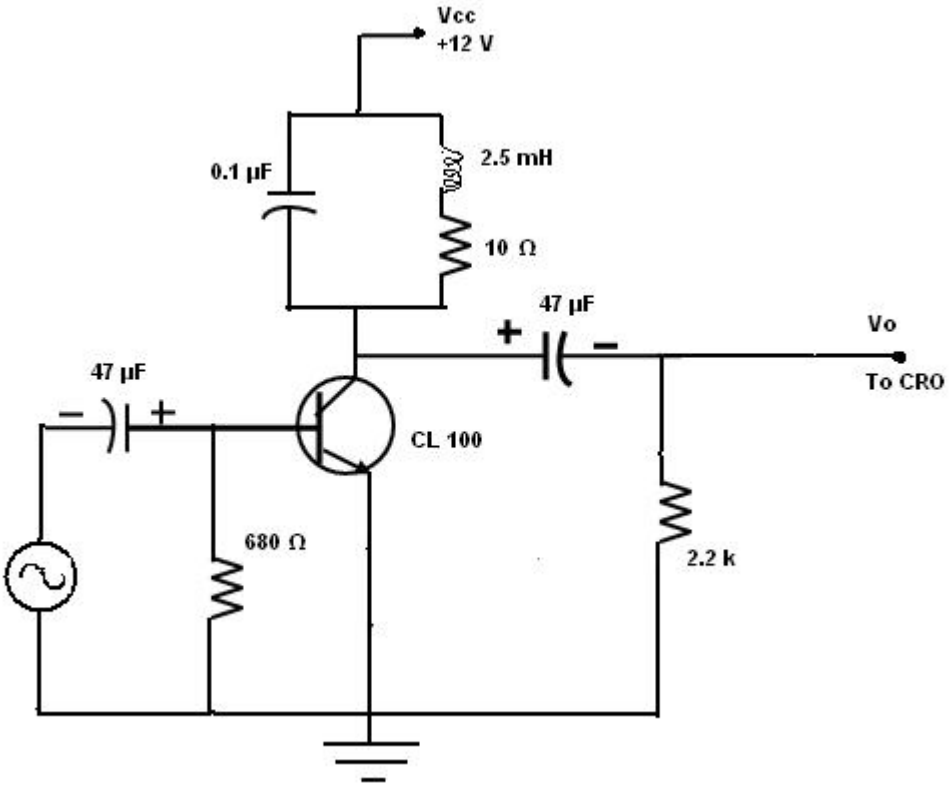
1. What is a monostable multivibrator?
2. State the applications of a monostable multivibrator.
3. What are the other names of a monostable multivibrator?
4. Why is monostable multivibrator also called as delay circuit?
5. What is the other name of monostable multivibrator?

RESULT:

Thus the monostable multivibrator has been designed to generate a pulse of duration **T**.
Theoretical pulse width T =
Practical pulse width T =

TUNED CLASS C AMPLIFIER

CIRCUIT DIAGRAM



MODEL GRAPH:

TUNED CLASS C AMPLIFIER

AIM:

To design and construct the class-c power amplifier and to plot its frequency response.

COMPONENTS REQUIRED:

S.NO	ITEM	RANGE	Q.TY
1	TRANSISTOR	BC 107	1
2	RESISTOR	4.2KΩ, 500Ω, 197KΩ, 2.2KΩ,	1
3	CAPACITOR	0.1μf 0.001μf, 100μf	2 1
4	CRO	-	1
5	RPS	(0-30) V	1
6	FUNCTION GENERATOR	-	1

THEORY:

In a class-c amplifier, the transistor is in the active region for less than half cycle. It means, conduction takes place for less than one half cycle. This implies that the collector current of a class-c amplifier is highly non-sinusoidal because current flows in pulses. The load is a tuned circuit which converts the non-sinusoidal o/p to nearly sinusoidal form. Because of the flow of collector current less than 180^0, the average collector current is much less, if hence losses are less, so efficiency is very high.

Resonance frequency (f_r)=$1/2\pi\sqrt{LC}$.

At resonant frequency, the inductance of parallel resonant circuit is very high and is purely resistive. When the circuit is tuned to the resonant frequency, the voltage across R_1 is maximum and sinusoidal. The tuned circuit helps in rejecting the harmonics that are developed in the transistor due to class-C operation.

The class-c tuned power amplifier consists of an LC tuned circuit in the collector of Q. R_1& R_2 provides the necessary biasing for Q. C_1& C_3 are the i/p and o/p coupling capacitors. The Q point is kept just above the cut-off line on the dc load line. R_L is provided to load the amplifier.

OBSERVATION:

V_{in}=____(v)

Frequency(Hz)	V_{out}(v)	Gain(dB)=20 log (V_0/V_{in})

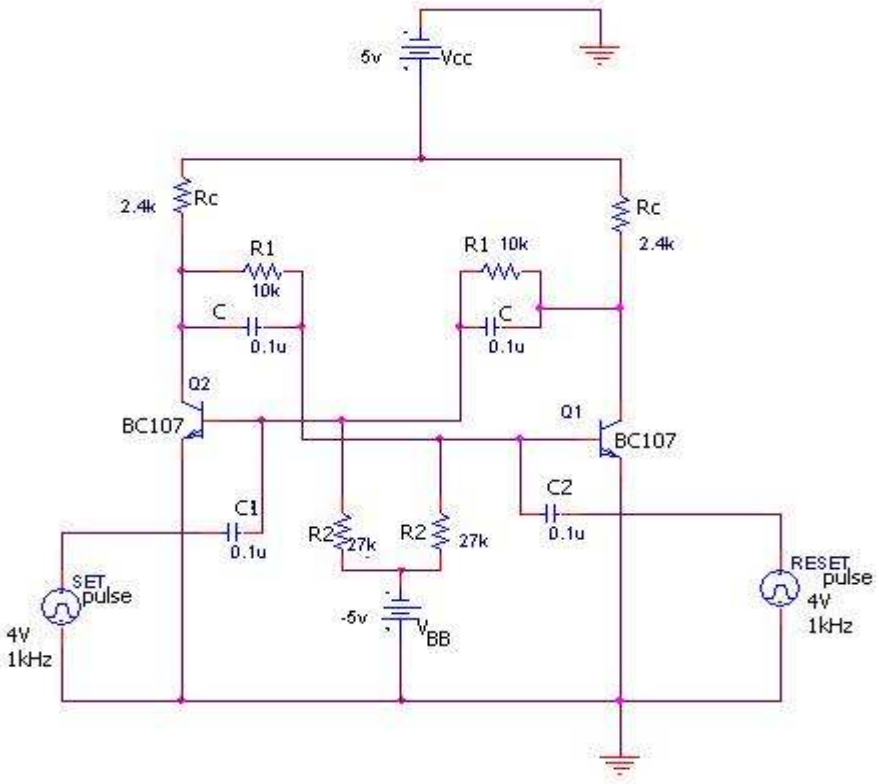
PROCEDURE:

1. Connect the circuit as for circuit diagram
2. Calculate the theoretical resonant frequency
   $f_r=1/2\prod\sqrt{LC}$.
3. Connect the i/p signal to the i/p of the amplifier.
4. Keep i/p voltage zero initially and adjust frequency to around resonance frequency (f_r)
5. Observe the o/p waveform increase the input ac voltage until we get the maximum distorted o/p.
6. Vary the frequency in required steps surrounding resonant frequency and note down the corresponding o/p voltages & calculate gain.
7. Plot the graph between gain and frequency.

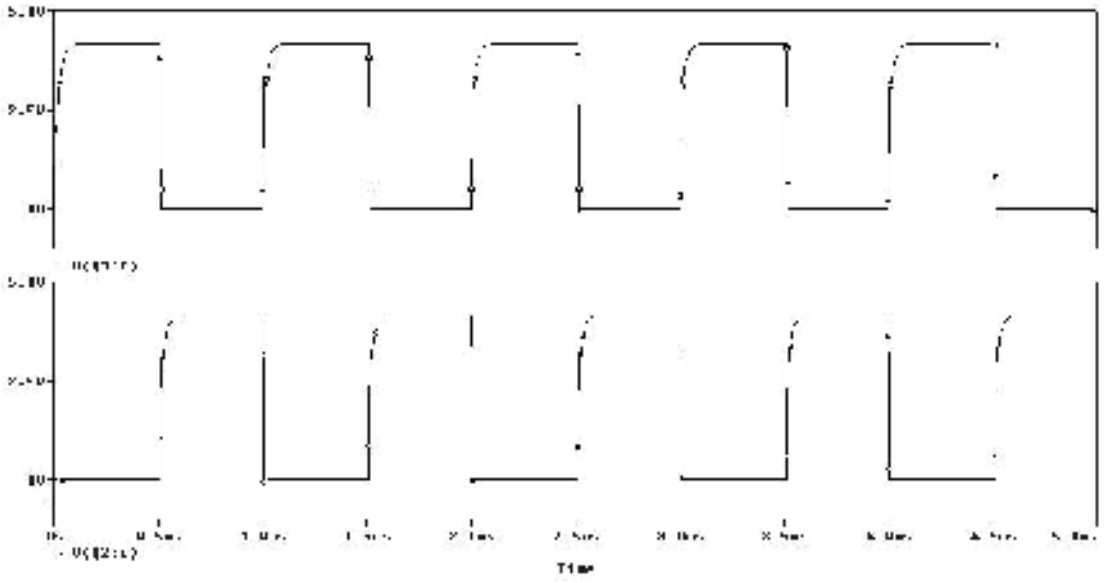
RESULT:

Thus single tuned amplifier is designed and constructed for the given operating frequency and the frequency response is plotted.

CIRCUIT DIAGRAM



MODEL GRAPH



BISTABLE MULTIVIBRATOR

AIM :

To observe the two stable state voltages in a bistable multivibrator using transistor.

APPARATUS REQUIRED:

S.No	COMPONENTS	RANGE/SPECIFICATION	QUANTITY
1	Resistor	10k Ω, 2.4kΩ, 27kΩ	2,2,2
2	Capacitor	0.1μF	4
3	AFG	(0-1)MHz	1
4	CRO	(0-30)MHz	1
5	Bread Board		1
6	NPN Transistor	BC107	2
7	Dual Power supply	(0 – 30 V)	1

DESIGN :

Vcc = 5V , V_{BB} = -5V ,$hfe_{(min)}$ = 20 , Ic =2mA , $V_{CE(sat)}$ =0.2V

$I_{C1} = (V_{CC} - V_{CE(sat)}) / Rc$

$Ic \approx I_{c2} = 2mA$

$Rc = (Vcc - V_{CE(sat)}) / I_{C2}$

$Rc = 2.4k\Omega$

$I4 = I_{C2} / 10 = 2mA / 10$

$I4 = 0.2mA$

$I4 = (V_{B2} + V_{BB}) / R2$

$R2 = 0.715 / 0.2mA$

$R2 = 28.5k\Omega$

Choose, R2 = 27 kΩ

$I_{B(min)} = Ic / hfe_{(min)} = 2mA / 20 = 0.1mA$

$I_{B2} = 1.5 * I_{B2(min)} = 0.15mA$

$I3 = I4 + I_{B2} = 0.2mA + 0.15mA = 0.35mA$

$I3 = (Vcc - VB2) / R1$

$R1 = 9.88kk\Omega$

Choose, $R1 = 10k\Omega$

Time period $T = 2C(R1 \parallel R2)$

Let $C = 0.1\mu F$, $T = 1.458ms$

PROCEDURE

1. Connect the circuit as per the circuit diagram.
2. Verify the stable states of Q1 and Q2
3. Apply the square wave of 4v p-p , 1KHz signal to the base of the transistor Q1.
4. Observe the wave forms at collectors of each transistors simultaneously.
5. Note down the time period and amplitude of the wave at the collector of the transistors Q1 and Q2.
6. Plot wave forms of Vc1 and Vc2 with respect to time in a linear graph.

REVIEW QUESTIONS :

1. What is meant by multivibrator ?
2. Distinguish oscillator and multivibrator .
3. List the applications of an bistable multivibrator .
4. What is a bistable multivibrator ?
5. What are the other names of a bistable multivibrator ?

RESULT:

Thus the two Stable state voltages in bistable multivibrator were observed.

Theoretical Time period =

Practical Time period =